ARBOR

ETXexpress Specification

Rev. 1.0

TONY

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1 Introduction

1.1 ETXexpress Specification and ETXexpress Design Guide

The Arbor ETXexpress Specification is based upon an open PICMG ® industry standard adopted for Computer-On-Modules. Please note that the ETXexpress Specification is exactly the same as the PICMG's® international COM Express™ Specification, which Arbor played a lead role in developing. All Arbor ETXexpress products are based on the COM Express™ Specification.

Arbor also has created an ETXexpress Design Guide specifically for its customers. There is no international PICMG® COM Express™ Design Guide.

The Arbor ETXexpress Design Guide, which is a different document than the ETXexpress Specification, also is available to Arbor customers upon request, explores the requirements of the ETXexpress Specification and provides recommendations on designing ETXexpress baseboards to support various features of ETXexpress modules. The ETXexpress Design Guide, based upon the ETXexpress Specification, discusses capabilities defined in the ETXexpress Specification with schematic examples where applicable and offers ideas to consider for maximum flexibility in designing baseboards.

1.2 ETXexpress COMs

An ETXexpress Computer-On-Module (COM) is a module with all components necessary for a bootable host computer, packaged as a super component. A COM requires a Carrier Board to bring out I/O and to power up. COMs are used to build single board computer solutions and offer OEMs fast time-to-market with reduced development cost. Like integrated circuits, they provide OEMs with significant freedom in meeting form-fit-function requirements. For all these reasons the COM methodology has gained much popularity with OEMs in the embedded industry.

The standard is designed to be future proof and to provide a smooth transition path from legacy parallel interfaces to LVDS (Low Voltage Differential Signaling) interfaces. These include the PCI bus and parallel ATA on the one hand and PCI Express and Serial ATA on the other hand.

Key features include:

- Rich complement of contemporary high bandwidth serial interfaces, including PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet
- 32-bit PCI, LPC and Parallel ATA options preserved for easy interface to a range of peripherals
- Extended power-management capabilities
- Robust thermal and mechanical concept
- Cost-effective design
- Legacy-free design (no Super I/O, PS2 keyboard or mouse)
- Compact module size with two footprint options to satisfy a range of performance requirements
- High-performance mezzanine connector with several pin-out types to satisfy a range of applications

The ETXexpress specification has been created to appeal to a range of vertical embedded markets. It has also been formulated to be applicable to a broad range of form factors, from floor-installed to bench-top to handheld. Markets and applications include but are not limited to:

- Healthcare - clinical diagnostic imaging systems, patient bedside monitors, etc.
- Retail & advertising - electronic shopping carts, billboards, kiosks, POS systems, etc.
- Test & measurement - scientific and industrial test and measurement instruments
- Gaming & entertainment - simulators, slot machines, etc.
- Industrial automation - industrial robots, vision systems, etc.
- Security - digital CCTV, luggage scanners, intrusion detectors, etc.
- Defense & government - unmanned vehicles, rugged laptops, wearable computers, etc.

Systems based on the ETXexpress Specification require the implementation of an application-specific Carrier Board that accepts the module. The Carrier Board is typically a 4- or 6-layer PCB. User-specific features such as external connector choices and locations and peripheral circuits can be tailored to suit the application. The OEM can focus on application-specific features rather than CPU board design. The OEM also benefits from a wide choice of modules providing a scalable range of price and performance upgrade options.

1.3 Objective

This specification defines ETXexpress modules at a level of detail sufficient to allow interoperability between independent vendors' modules and Carrier Boards.

1.4 Special Word Usage

- Mandatory features are indicated by the use of the word "**shall**."
- Recommended features are indicated by the use of the word "**should**."
- Optional features are indicated by the use of the word "**may**."

1.5 Acronyms / Definitions

Table 1-1: Terms and Definitions

Term	Definition
AC '97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – software standard to implement power saving modes in PC-AT systems
Basic Module	ETXexpress 125mm x 95mm module form factor.
BIOS	Basic Input Output System – acronym describing the firmware in PC-AT system that is used to initialize system components before handing control over to the operating system.
Carrier Board	An application specific circuit board that accepts a ETXexpress module.
CCTV	Closed Circuit Television
CVBS	Composite Video Baseband Signal
DDC	Display Data Control – VESA (Video Electronics Standards Association) standard to allow identification of the capabilities of a VGA monitor
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random Access Memory
DVI	Digital Visual Interface - a Digital Display Working Group (DDWG) standard that defines a standard video interface supporting both digital and analog video signals. The digital signals use DS.
EEPROM	Electrically Erasable Programmable Read-Only Memory
Extended Module	ETXexpress 155mm x 110mm module form factor.
FR4	A type of fiber-glass laminate commonly used for printed circuit boards.
Gb	Gigabit
GBE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
I^2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.
IDE	Integrated Device Electronics – parallel interface for hard disk drives – also known as PATA
Legacy Device	Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice. Definitions vary as to what constitutes a legacy device. Some definitions include IDE as a legacy device.
LAN	Local Area Network
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LS	Least Significant
LVDS	Low Voltage Differential Signaling – widely used as a physical interface for TFT flat panels. LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications.
MS	Most Significant
NA	Not Available
NC	No Connect
NTSC	National Television Standards Committee – video broadcast standard used in North America
OEM	Original Equipment Manufacturer
PAL	Phase Alternating Line – video broadcast standard used in many European countries.
PATA	Parallel AT Attachment – parallel interface standard for hard-disk drives – also known as IDE, AT Attachment, and as ATA
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s

Term	Definition
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PCI Express PCIE	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PEG	PCI Express Graphics
PHY	Ethernet controller physical layer device
Pin-out Type	A reference to one of five ETXexpress definitions for what signals appear on the ETXexpress module connector pins.
PS2 PS2 Keyboard PS2 Mouse	"Personal System 2" - an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s. The term survives as a reference to the style of mouse and keyboard interface that were introduced with the PS2 system.
R_a	Roughness Average – a measure of surface roughness, expressed in units of length.
ROM	Read Only Memory – a legacy term – often the device referred to as a ROM can actually be written to, in a special mode. Such writable ROMs are sometimes called Flash ROMs. BIOS is stored in ROM or Flash ROM.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SAS	Serial Attached SCSI – high speed serial version of SCSI
SCSI	Small Computer System Interface – an interface standard for high end disk drives and other computer peripherals
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM module configuration information
SO-DIMM	Small Outline Dual In-line Memory Module
S0, S1, S2, S3, S4, S5	System states describing the power and activity level S0 Full power, all devices powered S1 S2 S3 Suspend to RAM System context stored in RAM; RAM is in standby S4 Suspend to Disk System context stored on disk S5 Soft Off Main power rail off, only standby power rail present
SATA	Serial AT Attachment: serial-interface standard for hard disks
SDVO	Serialized Digital Video Output – Intel defined format for digital video output that can be used with Carrier Board conversion ICs to create parallel, DS, and LVDS flat-panel formats as well as NTSC and PAL TV outputs
SM Bus	System Management Bus
Super I/O	An integrated circuit, typically interfaced via the LPC bus that provides legacy PC I/O functions including PS2 keyboard and mouse ports, serial and parallel port(s) and a floppy interface.
TFT	Thin Film Transistor – refers to technology used in active matrix flat-panel displays, in which there is one thin film transistor per display pixel.
DS	Transition Minimized Differential Signaling - a digital signaling protocol between the graphics subsystem and display. DS is used for the DVI digital signals.
USB	Universal Serial Bus
VGA	Video Graphics Adapter – PC-AT graphics adapter standard defined by IBM.
WDT	Watch Dog Timer.
XAUI	10 Gigabit / sec Attachment Unit Interface.

1.6 Applicable Documents and Standards

The following publications are used in conjunction with this standard. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/
- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/
- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/
- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/
- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/labs/media/audio/
- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org/summary/sumddcci.h
- ExpressCard Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. http://www.expresscard.org/
- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications." http://www.ieee.org
- IEEE 802.3ae (Amendment to IEEE 802.3-2002), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.h
- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/

- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/
- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc, Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. http://www.usb.org/

2 Module Overview

2.1 Module Configuration

Two module sizes are defined: the Basic Module and the Extended Module. The primary difference between the Basic Module and the Extended Module is the over-all physical size and the performance envelope supported by each. The Extended Module is larger and can support larger processor and memory solutions. The Basic Module and Extended Module use the same connectors and pin-outs and utilize several common mounting hole positions. This level of compatibility allows that a carrier board designed to accommodate an Extended Module can also support a Basic Module.

Up to 440 pins of connectivity are available between ETXexpress modules and the Carrier Board. Legacy buses such as PCI, parallel ATA, LPC, AC'97 can be supported as well as new high speed serial interconnects such as PCI Express, Serial ATA or SAS and Gigabit Ethernet. To enhance interoperability between ETXexpress modules and Carrier Boards, five common signaling configurations (Pin-out Types) have been defined to ease system integration. Some Pin-out Types definitions require only a single 220-pin connector and others require both 220-pin connectors to supply all the defined signaling. All Pin-out Type definitions apply to either Basic Module or Extended Module sizes.

2.2 Feature Overview — Basic Module

The Basic Module is intended for mobile systems and space-constrained stationary systems. Key features of the Basic Module include:

- Module size: 125 mm x 95 mm
- 5mm and 8 mm stack height options (module bottom to Carrier Board top)
- 18 mm ‘z’ height with heat-spreader (with 5 mm stack option)
- Accommodates a single horizontal mount SO-DIMM
- Single 220 pin or dual 220 pin connectors for up to 440 pins

2.3 Feature Overview — Extended Module

The Extended Module, which targets OEM applications that require larger amounts of system memory, features a larger module size to accommodate full size DIMMs and larger chipsets and CPUs.

The key features of the Extended Module include:

- Module size: 155 mm x 110 mm
- 5mm and 8 mm stack height options (module bottom to Carrier Board top)
- 18 mm ‘z’ height with heat-spreader (with 5 mm stack option)
- Accommodates 2 full-size DIMM or mini DIMM memories or 2 right-angle mount or vertical mount SO-DIMMs
- Single 220 pin or dual 220 pin connectors for up to 440 pins
- Allows for the use of higher performance CPUs that can not be supported on the Basic Module

2.4 Feature Overview — Pin-out Type 1

- Single 220 pin connector (A-B connector)
- Up to 8 USB 2.0 ports; 4 shared over-current lines
- Up to 4 Serial ATA or SAS ports
- Up to 6 PCI Express lanes
- Support pins for up to 2 ExpressCards
- Dual 24-bit LVDS channels
- Analog VGA
- TV Out: Composite Video, S-Video, Component Video (YP_bP_r)
- AC '97 digital audio interface (external CODEC)
- Single Ethernet interface with integrated PHY – pinned for Gigabit Ethernet
- LPC interface
- 8 GPIO pins
- 120W maximum input power over module connector pins
- +12V primary power supply input
- +5V standby and 3.3V RTC power supply inputs

2.5 Feature Overview — Pin-out Type 2

- All Pin-out Type 1 features plus the following:
- Dual 220 pin connectors (A-B and C-D, 440 pins total)
- 32 bit PCI interface
- IDE port (to support legacy ATA devices such as CD-ROM drives and Compact Flash storage cards)
- Up to 22 PCI Express lanes (up to 6 on A-B and up to 16 on C-D)
- 16 of 22 PCI Express lanes commonly used for PCI Express Graphics
- SDVO option (pins shared with PCI Express Graphics)
- Maximum module input power capability extended to 188W

2.6 Feature Overview — Pin-out Type 3

All Pin-out Type 2 features with the exception of the following:

- IDE pins are reallocated to provide additional Gigabit Ethernet capability: no IDE
- Up to 3 Gigabit Ethernet channels
- Option to implement 10 Gigabit Ethernet channel instead of additional 2 Gigabit Ethernet ports

2.7 Feature Overview — Pin-out Type 4

All Pin-out Type 2 features with the exception of the following:

- PCI pins are reallocated to provide additional PCI Express lanes: no PCI
- Up to 32 PCI Express lanes

2.8 Feature Overview — Pin-out Type 5

All Pin-out Type 2 features with the exception of the following:

- Both IDE and PCI pins are reallocated: no IDE and no PCI
- Up to 32 PCI Express lanes
- Up to 3 Gigabit Ethernet channels
- Option to implement 10 Gigabit Ethernet channel instead of two additional Gigabit Ethernet ports

3 Required and Optional Features

3.1 Module Pin-out Type Definitions

Five pin-out types are defined. Pin-out Type 1 modules have a single 220-pin connector, the A-B connector. Module Pin-out Types 2 through 5 use a pair of 220 pin connectors, designated A-B and C-D, for a total of 440 pins. The variations in Pin-out Type definitions are summarized in the table below.

Table 3-1: Module Pin-out Type Overview

Types	Connector Rows	PCI Express Lanes	PCI	IDE Ports	LAN Ports
Type 1	A-B	Up to 6	-	-	1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit	-	3
Type 4	A-B C-D	Up to 32	-	1	1
Type 5	A-B C-D	Up to 32	-	-	3

For module Pin-out Types 2 through 5, a subset of the PCI Express lanes are commonly used as PCI Express Graphics (PEG) lanes. SDVO functions **may** be pin-shared with PEG lanes.

Type 1 modules allow for a minimal possible feature set using two of the four available connector rows. Type 1 represents a basic feature set with the benefit of simplified routing of the Carrier Board to allow a lower layer count board.

Type 2 modules include PCI and IDE interfaces. These modules either use on board graphics capabilities or **may** use 16 PEG lanes to connect to an external video controller. In case of on board graphics, PEG pins **may** be alternatively used for two SDVO ports.

Type 3 modules trade IDE port pins for two additional LAN ports, allowing up to three GBE interfaces, or one GBE and one 10 Gigabit LAN interface.

Type 4 modules drop the PCI interface, to allow up to 32 PCI Express lanes for applications with large I/O bandwidth requirements. IDE support is still available.

Type 5 modules trade IDE and PCI pins for up to 32 PCI Express lanes and up to three GBE interfaces, or one GBE and one 10 Gigabit LAN interface. These modules are intended for applications with large I/O bandwidth requirements.

3.2 Module Pin-out Types 1-5 — Required and Optional Features

ETXexpress Required and Optional features are summarized in the following table. The features identified as Minimum (Min.) **shall** be implemented by all modules. Features identified up to Maximum (Max) **may** be additionally implemented by a module.

Table 3-2: Module Pin-out Types 1-5 — Required and Optional Features

	Type 1 (Single connector) Min / Max	Type 2 Min / Max	Type 3 (No IDE) Min / Max	Type 4 (No PCI) Min / Max	Type 5 (No IDE, No PCI) Min / Max	Note
System I/O						
PCI Express Graphics (PEG)	NA	0 / 1	0 / 1	0 / 1	0 / 1	1
PCI Express Lanes 0 - 5	2 / 6	2 / 6	2 / 6	2 / 6	2 / 6	2
PCI Express Lanes 6-15	NA	NA	NA	0 / 10	0 / 10	2
PCI Express Lanes 16-31 (same as PEG pins)	NA	0 / 16	0 / 16	0 / 16	0 / 16	2
SDVO Channels	NA	0 / 2	0 / 2	0 / 2	0 / 2	3
LVDS Channels	0 / 2	0 / 2	0 / 2	0 / 2	0 / 2	4
VGA Port	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	5
TV-Out	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	6
PATA Port	NA	1 / 1	NA	1 / 1	NA	7
SATA / SAS Ports	2 / 4	2 / 4	2 / 4	2 / 4	2 / 4	8
AC'97 Digital Interface	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	9
USB 2.0 Ports	4 / 8	4 / 8	4 / 8	4 / 8	4 / 8	10
LAN 0 (10/100Base-T min)	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	11
LAN 1 (10/100Base-T min)	NA	NA	0 / 1	NA	0 / 1	11
LAN 2 (10/100Base-T min)	NA	NA	0 / 1	NA	0 / 1	11
PCI Bus - 32 Bit	NA	1 / 1	1 / 1	NA	NA	12
Express Card Support	1 / 2	1 / 2	1 / 2	1 / 2	1 / 2	13
LPC Bus	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	14
System Management						
General Purpose Inputs	4 / 4	4 / 4	4 / 4	4 / 4	4 / 4	15
General Purpose Outputs	4 / 4	4 / 4	4 / 4	4 / 4	4 / 4	15
SMBus	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	16
I^2C	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	17
Watch Dog Timer	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	18
Speaker Out	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	19
External BIOS ROM support	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	20
Reset Functions	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	21
Power Management						
Thermal Protection	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	22
Battery Low Alarm	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	23
Suspend	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	24
Wake	0 / 2	0 / 2	0 / 2	0 / 2	0 / 2	25
Power Button Support	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	26
Power Good	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	27

Notes for Table 3-2:

1. PCI Express Graphics (PEG). These signals **may** be multiplexed with SDVO signals or defined as ordinary PCI Express signals. The PEG lanes are the same lanes as PCI Express lanes 16-31.
2. The number of available PCI Express lanes varies with the module Pin-out Type. If the module supports off-module x16 PCI Express Graphics, then PCI Express Lanes 16-31 **shall** be used to implement this.
3. SDVO. Serial Digital Video Output to LVDS or DS transmitters on the Carrier Board. These signals, if implemented, **shall** be multiplexed with PEG signals.
4. LVDS. Low voltage differential signaling flat-panel interface. The module pin-out allows two single channel display interfaces (each with 1 pixel per clock) with up to 24 bits per color. Alternatively, one dual channel display (2 pixels per clock) with up to 24 bits per color, 48 bits per clock is allowed. Includes panel backlight control and EDID support.
5. VGA. Analog RGB interface for CRT monitor and DDC support.
6. If TV-Out is supported, then Composite Video **shall** be available. Component and S-Video **may** also be available.
7. PATA. Parallel ATA support for up to 2 devices in a master/slave configuration. This signaling interface is limited to ATA100 speeds. Higher (ATA133) speeds are not defined. PATA signal pins are reused in Pin-out Type 3 and 5 modules for 2 additional GB Ethernet interfaces.
8. SATA / SAS. Serial ATA links for support of existing SATA-150 and emerging SATA-300 devices. Alternatively, this interface **may** be used for Serial Attached SCSI (SAS). SAS operation **may** be indicated by a byte in the Carrier Board configuration EE-PROM (see Section 5.3).
9. AC ’97. The AC ’97 audio codec interface is limited to support a single AC ’97 link. High Definition Audio **may** be supported.
10. USB. All USB interfaces **shall** be USB 2.0 compliant. The minimum of 4 USB channels provides support for keyboard, mouse, CD/DVD drive, and one additional device. Note that this usage is not required and the actual carrier usage of the USB port is undefined by this specification.
11. LAN. Up to 3 Gigabit Ethernet ports are defined, designated GBE0 through GBE2. The ports **may** operate in 10, 100, or 1000 Mbit/sec modes. The ports are analog-encoded GBE signals, post PHY but without isolation magnetics. Magnetics are assumed to be on the Carrier Board. All ETXexpress modules **shall** implement at least one 10/100 Ethernet port on the GBE0 pin slot. Ports GBE1 and GBE2 **may** be combined to form a 10 Gigabit / sec Ethernet interface.
12. PCI. The PCI bus interface is specified to be a 32-bit PCI 2.3 compliant bus with speed options of 33MHz or 66MHz.
13. ExpressCard is a small form factor expansion card for mobile systems that uses PCI Express or USB as the interface. It is similar in concept and scope to CardBus. ETXexpress modules **shall** provide support functions for at least one ExpressCard. This does not mean that a module PCI Express lane or USB link are specifically allocated to ExpressCard use, but it does mean that the module pins for ExpressCard detection and support are present.
14. LPC bus. The LPC bus provides legacy I/O support on a Carrier Board via a Super I/O and system-management devices.
15. General Purpose Input and Output pins. GPI and GPO pins **may** be implemented as GPIO (module specific).

16. SMBus. The SMBus port is specified for system management functions. It is used on the module to mange system functions such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters. Off module, the SMBus **should** be used carefully. It **may** be useful for implementation on the Carrier Board of standards such as Smart Battery.
17. I^2C. The I^2C port **shall** be available in addition to the SMBus.
18. Watch Dog Timer (WDT). Refer to Section 5.8 for details.
19. Speaker Out. This port provides the PC beep signal and is mostly intended for debugging purposes.
20. External BIOS ROM. A module pin, BIOS_DISABLE#, **may** be provided by the module hardware. If the function is supported, then the Carrier Board **may** pull the BIOS_DISABLE# pin low to disable the on-module BIOS ROM, allowing the module to boot from a BIOS ROM implemented on the Carrier Board.
21. Resets. This function includes reset signals to and from the module. Signals SYS_RESET#, CB_RESET# and KBD_RST# **shall** be supported for all module pin-out types. Signal PCI_RESET# **shall** be supported for pin-out types 2 and 3. Signal IDE_RESET# **shall** be supported for pin-out types 2 and 4. Additionally, signal PWR_OK **should** be an input term that keeps the module in a reset condition if low.
22. Thermal Protection. This port provides thermal signaling to protect critical components on the module and the Carrier Board.
23. Battery Low Alarm. This port provides a battery-low signal to the module for orderly transitioning to power saving or power cut-off ACPI modes.
24. Suspend. This port defines the signaling to indicate that the module has entered the ACPI power-saving mode S3 (Suspend-To-RAM or STR), S4 (Suspend-To-Disk or STD), or S5 (Soft-Off).
25. Wake. This port defines the signaling to wake up the module from a power saving mode. Most prevalent choices for these signals are RING# and LID#, although other choices can be implemented.
26. Power Button. This port defines the signaling for powering down the module.
27. Power Good. This port defines the signaling for the correct power conditions to proceed with normal startup of the module.

3.3 ETXexpress Module Feature Fill Order

ETXexpress allows a variable number of ports to be implemented for several interfaces, per Table 3-2 above. Ports **shall** be populated in a “low to high” manner, per the following table.

Table 3-3: Module Feature Fill Order

Feature	Number of Ports	Fill Order
Express Card Support	1	EXCD 0
	2	EXCD 0,1
LAN	1	GBE channel 0
	2	GBE channels 0,1
	3	GBE channels 0,1,2
LVDS	1	LVDS channel A
	2	LVDS channels A,B
SATA / SAS	2	SATA / SAS channels 0,1
	3	SATA / SAS channels 0,1,2
	4	SATA / SAS channels 0,1,2,3
SDVO	1	SDVO channel B
	2	SDVO channels B,C
USB	4	USB channels 0,1,2,3
	5	USB channels 0,1,2,3,4
	6	USB channels 0,1,2,3,4,5
	7	USB channels 0,1,2,3,4,5,6
	8	USB channels 0,1,2,3,4,5,6,7

The ETXexpress PCI Express lanes also have a prescribed fill order, described in Section 5.2, “PCI Express Link Configuration Guidelines.”

4 Signal Descriptions

4.1 Signal Naming Convention

Active-low signals are indicated by a trailing '#' sign:	REQ#
Differential pairs are indicated by trailing '+' and '-' signs:	TX+, TX-
Bused signals are indicated by brackets, with LS bit first, MS bit last:	A[0:31]
Bus brackets **may** appear anywhere in the signal name:	CBE[0:3]#

4.2 Pin and Signal Buffer Types

Pin and Buffer type definitions apply to the signals in the Signal List section below.

4.2.1 *Pin Types*

I	Input to the module
O	Output from the module
I/O	Bi-directional input / output signal
OD	Open drain output

4.2.2 *Buffer Types*

CMOS Logic input or output. Input thresholds and output levels **shall** be 80% of supply rail for high side and 20% of the relevant supply rail for low side.

PCIE PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (module outputs) **shall** be AC coupled on the module. PCIE receive pins (module inputs) **shall** be DC coupled on the ETXexpress module and **shall** be assumed to be AC coupled off-module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the module PCIE receive lanes (target PCIE device transmit lanes) **shall** be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals **shall** be AC coupled on the add-in card, not on the Carrier Board.

PCI PCI 2.3 compatible signal. Please refer to the PCI Rev. 2.3 Specification for details.

SATA SATA compatible differential signal. Please refer to the SATA Specification for details. All ETXexpress SATA signals **shall** be AC coupled on the module

LVDS Low Voltage Differential Signal – 330mV nominal; 450mV maximum differential signal.

USB USB 2.0 compatible differential signal. Please refer to the USB 2.0 Specification for details.

REF Reference voltage output. **May** be sourced from a module power plane.

PDS Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities to the Carrier Board.

Analog Inputs and Outputs used for LAN, VGA and TV OUT are analog signals.

Power Inputs used for power delivery to the module electronics.

4.2.3 *Power Rails and Tolerances*

Pins are marked in the following table with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different. For example, the PCI group is defined as having a 3.3V power rail, meaning that the output signals will only be driven to 3.3V, but the pins are tolerant of 5V signals.

An additional label, “Suspend” indicates that the pin is active during suspend states (S3,S4,S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

4.3 Signal List

ETXexpress signal descriptions are described in the following table. The Pin Availability column in the table indicates in which Pin-out Types the signal is available. Module Pin-out Types 1 through 5 are designated T1,T2,T3,T4,T5 in the Pin Availability column. A notation of “All” indicates that the signal is available to all module Pin-out Types.

Table 4-1: Signals, Pin Types, and Descriptions

AC97 Audio / High Definition Audio	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
AC_RST#	O CMOS	3.3V / 3.3V Suspend	Reset output to AC97 CODEC, active low.	All
AC_SYNC	O CMOS	3.3V / 3.3V	48kHz fixed-rate, sample-synchronization signal to the CODEC(s).	All
AC_BITCLK	I/O CMOS	3.3V / 3.3V	12.228 MHz serial data clock generated by the external CODEC(s).	All
AC_SDOUT	O CMOS	3.3V / 3.3V	Serial TDM data output to the CODEC.	All
AC_SDIN[0:2]	I CMOS	3.3V / 3.3V Suspend	Serial TDM data inputs from up to 3 CODECs.	All

Gigabit Ethernet	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	I/O Analog	3.3V max Suspend	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- : B1_DA+/- : TX+/- : TX+/- MDI[1]+/- : B1_DB+/- : RX+/- : RX+/- MDI[2]+/- : B1_DC+/- MDI[3]+/- : B1_DD+/-	All
GBE0_ACT#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 0 activity indicator, active low.	All
GBE0_LINK#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 0 link indicator, active low.	All
GBE0_LINK100#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	All
GBE0_LINK1000#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	All
GBE0_CTREF	REF	GND min 3.3V max	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output **shall** be current limited on the module. In the case in which the reference is shorted to ground, the current **shall** be limited to 250 mA or less.	All

Signal Descriptions

Gigabit Ethernet	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GBE1_MDI[0:3]+ GBE1_MDI[0:3]-	I/O Analog	3.3V max Suspend	Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/- This set of differential pairs, in conjunction with the GBE2_MDI[0:3] pairs, **may** also be used to implement a 10 Gigabit / sec interface, as described in Section 5.7 of this document.	T3,T5
GBE1_ACT#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 1 activity indicator, active low.	T3,T5
GBE1_LINK#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 1 link indicator, active low.	T3,T5
GBE1_LINK100#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 1 100 Mbit / sec link indicator, active low.	T3,T5
GBE1_LINK1000#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 1 1000 Mbit / sec link indicator, active low.	T3,T5
GBE2_MDI[0:3]+ GBE2_MDI[0:3]-	I/O Analog	3.3V max Suspend	Gigabit Ethernet Controller 2: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/- This set of differential pairs, in conjunction with the GBE1_MDI[0:3] pairs, **may** also be used to implement a 10 Gigabit / sec interface, as described in Section 5.7 of this document.	T3,T5
GBE2_ACT#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 2 activity indicator, active low.	T3,T5
GBE2_LINK#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 2 link indicator, active low.	T3,T5
GBE2_LINK100#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 2 100 Mbit / sec link indicator, active low.	T3,T5
GBE2_LINK1000#	OD CMOS	3.3V / 3.3V Suspend	Gigabit Ethernet Controller 2 1000 Mbit / sec link indicator, active low.	T3,T5
GBE2_CTREF	REF	GND min 3.3V max	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output **shall** be current limited on the module. In the case in which the reference is shorted to ground, the current **shall** be 250 mA or less.	T3,T5

IDE	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
IDE_D[0:15]	I/O CMOS	3.3V / 5V	Bidirectional data to / from IDE device.	T2, T4
IDE_A[0:2]	O CMOS	3.3V / 3.3V	Address lines to IDE device.	T2, T4
IDE_IOW#	O CMOS	3.3V / 3.3V	I/O write line to IDE device. Data latched on trailing (rising) edge.	T2, T4
IDE_IOR#	O CMOS	3.3V / 3.3V	I/O read line to IDE device.	T2, T4
IDE_REQ	I CMOS	3.3V / 5V	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	T2, T4
IDE_ACK#	O CMOS	3.3V / 3.3V	IDE Device DMA Acknowledge.	T2, T4
IDE_CS1#	O CMOS	3.3V / 3.3V	IDE Device Chip Select for 1F0h to 1FFh range.	T2, T4
IDE_CS3#	O CMOS	3.3V / 3.3V	IDE Device Chip Select for 3F0h to 3FFh range.	T2, T4
IDE_IORDY	I CMOS	3.3V / 5V	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	T2, T4
IDE_RESET#	O CMOS	3.3V / 3.3V	Reset output to IDE device, active low.	T2, T4
IDE_IRQ	I CMOS	3.3V / 5V	Interrupt request from IDE device.	T2, T4
IDE_CBLID#	I CMOS	3.3V / 5V	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	T2, T4

Serial ATA	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SATA0_TX+ SATA0_TX-	O SATA	AC coupled on module	Serial ATA or SAS Channel 0 transmit differential pair.	All
SATA0_RX+ SATA0_RX-	I SATA	AC coupled on module	Serial ATA or SAS Channel 0 receive differential pair.	All
SATA1_TX+ SATA1_TX-	O SATA	AC coupled on module	Serial ATA or SAS Channel 1 transmit differential pair.	All
SATA1_RX+ SATA1_RX-	I SATA	AC coupled on module	Serial ATA or SAS Channel 1 receive differential pair.	All
SATA2_TX+ SATA2_TX-	O SATA	AC coupled on module	Serial ATA or SAS Channel 2 transmit differential pair.	All
SATA2_RX+ SATA2_RX-	I SATA	AC coupled on module	Serial ATA or SAS Channel 2 receive differential pair.	All
SATA3_TX+ SATA3_TX-	O SATA	AC coupled on module	Serial ATA or SAS Channel 3 transmit differential pair.	All
SATA3_RX+ SATA3_RX-	I SATA	AC coupled on module	Serial ATA or SAS Channel 3 receive differential pair.	All
ATA_ACT#	O CMOS	3.3V / 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.	All

Signal Descriptions

PCI Express Lanes (General Purpose)	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PCIE_TX[0:5]+ PCIE_TX[0:5]-	O PCIE	AC coupled on module	PCI Express Differential Transmit Pairs 0 through 5	All
PCIE_RX[0:5]+ PCIE_RX[0:5]-	I PCIE	AC coupled off module	PCI Express Differential Receive Pairs 0 through 5	All
PCIE_TX[6:15]+ PCIE_TX[6:15]-	O PCIE	AC coupled on module	PCI Express Differential Transmit Pairs 6 through 15	T4, T5
PCIE_RX[6:15]+ PCIE_RX[6:15]-	I PCIE	AC coupled off module	PCI Express Differential Receive Pairs 6 through 15	T4, T5
PCIE_TX[16:31]+ PCIE_TX[16:31]-	O PCIE	AC coupled on module	PCI Express Differential Transmit Pairs 16 through 31 These are same lines as PEG_TX[0:15]+ and -	T2, T3, T4, T5
PCIE_RX[16:31]+ PCIE_RX[16:31]-	I PCIE	AC coupled off module	PCI Express Differential Receive Pairs 16 through 31 These are the same lines as PEG_RX[0:15]+ and -	T2, T3, T4, T5
PCIE_CLK_REF+ PCIE_CLK_REF-	O CMOS	3.3V / 3.3V	Reference clock output for all PCI Express and PCI Express Graphics lanes.	All

PCI Express Lanes x16 Graphics	Pin Type	Pwr Rail / Tolerance		Pin Availability
PEG_TX[0:15]+ PEG_TX[0:15]-	O PCIE	AC coupled on module	PCI Express Graphics transmit differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_TX[16:31]+ and - in module pin-out types 4 and 5.	T2, T3, T4, T5
PEG_RX[0:15]+ PEG_RX[0:15]-	I PCIE	AC coupled off module	PCI Express Graphics receive differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_RX[16:31]+ and - in module pin-out types 4 and 5.	T2, T3, T4, T5
PEG_LANE_RV#	I CMOS	3.3V / 3.3V	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this strap is low.	T2, T3, T4, T5
PEG_ENABLE#	I CMOS	3.3V / 3.3V	Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.	T2, T3, T4, T5

ExpressCard Support	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
EXCD[0:1]_CPPE#	I CMOS	3.3V / 3.3V	PCI ExpressCard: PCI Express capable card request, active low, one per card	All
EXCD[0:1]_RST#	O CMOS	3.3V / 3.3V	PCI ExpressCard: reset, active low, one per card	All

PCI Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PCI_AD[0:31]	I/O CMOS	3.3V / 5V	PCI bus multiplexed address and data lines	T2, T3
PCI_C/BE[0:3]#	I/O CMOS	3.3V / 5V	PCI bus byte enable lines, active low	T2, T3
PCI_DEVSEL#	I/O CMOS	3.3V / 5V	PCI bus Device Select, active low.	T2, T3
PCI_FRAME#	I/O CMOS	3.3V / 5V	PCI bus Frame control line, active low.	T2, T3
PCI_IRDY#	I/O CMOS	3.3V / 5V	PCI bus Initiator Ready control line, active low.	T2, T3
PCI_TRDY#	I/O CMOS	3.3V / 5V	PCI bus Target Ready control line, active low.	T2, T3
PCI_STOP#	I/O CMOS	3.3V / 5V	PCI bus STOP control line, active low, driven by cycle initiator.	T2, T3
PCI_PAR	I/O CMOS	3.3V / 5V	PCI bus parity	T2, T3
PCI_PERR#	I/O CMOS	3.3V / 5V	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	T2, T3
PCI_REQ[0:3]#	I CMOS	3.3V / 5V	PCI bus master request input lines, active low.	T2, T3
PCI_GNT[0:3]#	O CMOS	3.3V / 5V	PCI bus master grant output lines, active low.	T2, T3
PCI_RESET#	O CMOS	3.3V / 5V Suspend	PCI Reset output, active low.	T2, T3
PCI_LOCK#	I/O CMOS	3.3V / 5V	PCI Lock control line, active low.	T2, T3
PCI_SERR#	I/O OD CMOS	3.3V / 5V	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	T2, T3
PCI_PME#	I CMOS	3.3V / 5V Suspend	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	T2, T3
PCI_CLKRUN#	I/O CMOS	3.3V / 5V	Bidirectional pin used to support PCI clock run protocol for mobile systems.	T2, T3
PCI_IRQ[A:D]#	I CMOS	3.3V / 5V	PCI interrupt request lines.	T2, T3
PCI_CLK	O CMOS	3.3V / 3.3V	PCI 33MHz clock output.	T2, T3
PCI_M66EN	I CMOS	3.3V / 5V	Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation. If the module is not capable of supporting 66 MHz PCI operation, this input **may** be a no-connect on the module. If the module is capable of supporting 66 MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface **shall** operate at 33 MHz.	T2, T3

USB	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
USB[0:7]+ USB[0:7]-	I/O USB	3.3V / 3.3V Suspend	USB differential pairs, channels 0 through 7	All
USB_0_1_OC#	I CMOS	3.3V / 3.3V Suspend	USB over-current sense, USB channels 0 and 1. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_2_3_OC#	I CMOS	3.3V / 3.3V Suspend	USB over-current sense, USB channels 2 and 3. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_4_5_OC#	I CMOS	3.3V / 3.3V Suspend	USB over-current sense, USB channels 4 and 5. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_6_7_OC#	I CMOS	3.3V / 3.3V Suspend	USB over-current sense, USB channels 6 and 7. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low. Do not pull this line high on the Carrier Board.	All

LVDS Flat Panel	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
LVDS_A[0:3]+ LVDS_A[0:3]-	O LVDS		LVDS Channel A differential pairs	All
LVDS_A_CK+ LVDS_A_CK-	O LVDS		LVDS Channel A differential clock	All
LVDS_B[0:3]+ LVDS_B[0:3]-	O LVDS		LVDS Channel B differential pairs	All
LVDS_B_CK+ LVDS_B_CK-	O LVDS		LVDS Channel B differential clock	All
LVDS_VDD_EN	O CMOS	3.3V / 3.3V	LVDS panel power enable	All
LVDS_BKLT_EN	O CMOS	3.3V / 3.3V	LVDS panel backlight enable	All
LVDS_BKLT_CTRL	O CMOS	3.3V / 3.3V	LVDS panel backlight brightness control	All
LVDS_I2C_CK	O CMOS	3.3V / 3.3V	I^2C clock output for LVDS display use	All
LVDS_I2C_DAT	I/O OD CMOS	3.3V / 3.3V	I^2C data line for LVDS display use	All

LPC Interface	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
LPC_AD[0:3]	I/O CMOS	3.3V / 3.3V	LPC multiplexed address, command and data bus	All
LPC_FRAME#	O CMOS	3.3V / 3.3V	LPC frame indicates the start of an LPC cycle	All
LPC_DRQ[0:1]#	I CMOS	3.3V / 3.3V	LPC serial DMA request	All
LPC_SERIRQ	I/O CMOS	3.3V / 3.3V	LPC serial interrupt	All
LPC_CLK	O CMOS	3.3V / 3.3V	LPC clock output - 33MHz nominal	All

Analog VGA	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
VGA_RED	O Analog		Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	All
VGA_GRN	O Analog		Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	All
VGA_BLU	O Analog		Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	All
VGA_HSYNC	O CMOS	3.3V / 3.3V	Horizontal sync output to VGA monitor	All
VGA_VSYNC	O CMOS	3.3V / 3.3V	Vertical sync output to VGA monitor	All
VGA_I2C_CK	O CMOS	3.3V / 3.3V	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	All
VGA_I2C_DAT	I/O OD CMOS	3.3V / 3.3V	DDC data line.	All

TV Out	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
TV_DAC_A	O Analog		TVDAC Channel A Output supports the following: Composite video: CVBS Component video: Chrominance (Pb) analog signal S-Video: not used	All
TV_DAC_B	O Analog		TVDAC Channel B Output supports the following: Composite video: not used Component video: Luminance (Y) analog signal. S-Video: Luminance analog signal.	All
TV_DAC_C	O Analog		TVDAC Channel C Output supports the following: Composite video: not used Component: Chrominance (Pr) analog signal. S-Video: Chrominance analog signal.	All

Signal Descriptions

SDVO	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SDVOB_RED+ SDVOB_RED-	O PCIE	AC coupled on module	Serial Digital Video B red output differential pair Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair	Muxed with x16 PEG
SDVOB_GRN+ SDVOB_GRN-	O PCIE	AC coupled on module	Serial Digital Video B green output differential pair Multiplexed with PEG_TX[1]+ and PEG_TX[1]-	Muxed with x16 PEG
SDVOB_BLU+ SDVOB_BLU-	O PCIE	AC coupled on module	Serial Digital Video B blue output differential pair Multiplexed with PEG_TX[2]+ and PEG_TX[2]-	Muxed with x16 PEG
SDVOB_CK+ SDVOB_CK-	O PCIE	AC coupled on module	Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-	Muxed with x16 PEG
SDVOB_INT+ SDVOB_INT-	I PCIE	AC coupled off module	Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-	Muxed with x16 PEG
SDVOC_RED+ SDVOC_RED-	O PCIE	AC coupled on module	Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-	Muxed with x16 PEG
SDVOC_GRN+ SDVOC_GRN-	O PCIE	AC coupled on module	Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-	Muxed with x16 PEG
SDVOC_BLU+ SDVOC_BLU-	O PCIE	AC coupled on module	Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-	Muxed with x16 PEG
SDVOC_CK+ SDVOC_CK-	O PCIE	AC coupled on module	Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]-	Muxed with x16 PEG
SDVOC_INT+ SDVOC_INT-	I PCIE	AC coupled off module	Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]-	Muxed with x16 PEG
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I PCIE	AC coupled off module	Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-	Muxed with x16 PEG
SDVO_FLDSTALL+ SDVO_FLDSTALL-	I PCIE	AC coupled off module	Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-	Muxed with x16 PEG
SDVO_I2C_CK	O CMOS	2.5V / 2.5V	SDVO I^2C clock line - to set up SDVO peripherals.	T2, T3, T4, T5
SDVO_I2C_DAT	I/O OD CMOS	2.5V / 2.5V	SDVO I^2C data line - to set up SDVO peripherals.	T2, T3, T4, T5

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
I2C_CK	O CMOS	3.3V / 3.3V	General purpose I^2C port clock output	All
I2C_DAT	I/O OD CMOS	3.3V / 3.3V	General purpose I^2C port data I/O line	All
SPKR	O CMOS	3.3V / 3.3V	Output for audio enunciator - the "speaker" in PC-AT systems	All
BIOS_DISABLE#	I CMOS	3.3V / 3.3V	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.	All
WDT	O CMOS	3.3V / 3.3V	Output indicating that a watchdog time-out event has occurred.	All
KBD_RST#	I CMOS	3.3V / 3.3V	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	All
KBD_A20GATE	I CMOS	3.3V / 3.3V	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.	All

Power and System Management	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PWRBTN#	I CMOS	3.3V / 3.3V Suspend	Power button to bring system out of S5 (soft off), active on rising edge.	All
SYS_RESET#	I CMOS	3.3V / 3.3V Suspend	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.	All
CB_RESET#	O CMOS	3.3V / 3.3V Suspend	Reset output from module to Carrier Board. Active low. Issued by module chipset and **may** result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or **may** be initiated by the module software.	All
PWR_OK	I CMOS	3.3V / 3.3V	Power OK from main power supply. A high value indicates that the power is good.	All
SUS_STAT#	O CMOS	3.3V / 3.3V Suspend	Indicates imminent suspend operation; used to notify LPC devices.	All
SUS_S3#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Suspend to RAM state. Active low output.	All
SUS_S4#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Suspend to Disk state. Active low output.	All
SUS_S5#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.	All
WAKE0#	I CMOS	3.3V / 3.3V Suspend	PCI Express wake up signal.	All
WAKE1#	I CMOS	3.3V / 3.3V Suspend	General purpose wake up signal. **May** be used to implement wake-up on PS2 keyboard or mouse activity.	All
BATLOW#	I CMOS	3.3V / 3.3V Suspend	Indicates that external battery is low.	All
THRM#	I CMOS	3.3V / 3.3V	Input from off-module temp sensor indicating an over-temp situation.	All
THERMTRIP#	O CMOS	3.3V / 3.3V	Active low output indicating that the CPU has entered thermal shutdown.	All
SMB_CK	I/O OD CMOS	3.3V / 3.3V Suspend Rail	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	All
SMB_DAT	I/O OD CMOS	3.3V / 3.3V Suspend Rail	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	All
SMB_ALERT#	I CMOS	3.3V / 3.3V Suspend Rail	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	All

General Purpose I/O	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GPO[0:3]	O CMOS	3.3V / 3.3V	General purpose output pins. Upon a hardware reset, these outputs **should** be low.	All
GPI[0:3]	I CMOS	3.3V / 3.3V	General purpose input pins. Pulled high internally on the module.	All

Signal Descriptions

Module Type Definition	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
TYPE[0:2]#	PDS		The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pin-out Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pin-out Type 1 NC NC NC Pin-out Type 2 NC NC GND Pin-out Type 3 (no IDE) NC GND NC Pin-out Type 4 (no PCI) NC GND GND Pin-out Type 5 (no IDE, no PCI) The Carrier Board **should** implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic **may** also implement a fault indicator such as an LED.	T2, T3, T4, T5

Power and GND	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
VCC_12V	Power		Primary power input: +12V nominal. See Electrical Specifications section for allowable input range. All available VCC_12V pins on the connector(s) **shall** be used.	All
VCC_5V_SBY	Power		Standby power input: +5.0V nominal. See Electrical Specifications section for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) **shall** be used. Only used for standby and suspend functions. **May** be left unconnected if these functions are not used in the system design.	All
VCC_RTC	Power		Real-time clock circuit-power input. Nominally +3.0V. See Electrical Specifications section for details.	All
GND	Power		Ground - DC power and signal and AC signal return path. All available GND connector pins **shall** be used and tied to Carrier Board GND plane.	All

4.4 Signals Requiring Carrier Board Termination

Some signals, detailed below, require Carrier Board termination for proper operation. If the signals and the feature are not used, no Carrier Board termination is required, and the pins **may** be left open.

4.4.1 *Ethernet*

External Ethernet magnetics **shall** be implemented on the Carrier Board.

4.4.2 *Analog VGA*

If analog VGA is used, the VGA_RED, VGA_GRN, and VGA_BLU signals **shall** each be terminated on the Carrier Board through a 150 ohm resistor to ground. These resistors **should** be placed close to the VGA connector on the Carrier Board. These lines **may** be left unterminated if the analog VGA function is not used.

4.4.3 *TV Out*

If TV Out is used, the TV_DAC_A, TV_DAC_B, and TV_DAC_C lines **shall** be terminated on the Carrier Board through a 150-ohm resistor to ground. The termination resistors **should** be placed close to the external TV-Out connector(s). These lines **may** be left un-terminated if the TV Out function is not used.

4.4.4 *LVDS*

The LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) **shall** have 100-ohm terminations across the pairs at the destination. This **may** be on the Carrier Board, if the Carrier Board implements a LVDS de-serializer on-board.

Unused LVDS lines **may** be left open.

4.4.5 *USB*

No termination is required on USB pairs. A common mode choke is advisable if USB pairs on the Carrier Board are routed to a connector for use with an external cable.

Signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# are used to flag a USB over-current situation. Carrier Board USB current monitors **may** pull these lines to GND with open drain drivers to indicate that the monitor's current limit has been exceeded. Do not pull up these lines to 3.3V on the Carrier Board – this **shall** be done on the module.

4.4.6 *SDVO*

When implementing SDVO devices on the Carrier Board, the SDVO_CLK and SDVO_DATA lines **shall** have pull-up resistors to 2.5V +/- 5%. The resistor value **should** be 3.5K. When implementing slots for SDVO cards on the Carrier Board, the pull-up resistors **shall not** be placed on the Carrier Board because add-on SDVO cards have pull-up resistors. The pull-up resistors on the SDVO_CLK and SDVO_DATA allow the module chipset to determine that the pins shared between PCI Express Graphics and SDVO are to be used for SDVO.

4.5 Pin-out Tables for Types 1–5

Pin-out information for module pin-out Types 1–5 is provided in the five tables on the following pages.

Table 4-2: Pin List for Pin-out Type 1

Module Pin-out Type 1 implements a single 220 pin connector and a minimal feature set including up to 6 PCI Express lanes, up to 8 USB, up to 4 SATA, LPC, LVDS, analog VGA, TV-Out, power management and miscellaneous functions. Modules implementing Pin-out Type 1 **shall** use the pin-out shown in this table. Refer to Table 3-2 for minimum requirements and Table 3-3 for the order in which interfaces **shall** be implemented.

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)				
A2	GBE0_MDI3-	B2	GBE0_ACT#				
A3	GBE0_MDI3+	B3	LPC_FRAME#				
A4	GBE0_LINK100#	B4	LPC_AD0				
A5	GBE0_LINK1000#	B5	LPC_AD1				
A6	GBE0_MDI2-	B6	LPC_AD2				
A7	GBE0_MDI2+	B7	LPC_AD3				
A8	GBE0_LINK#	B8	LPC_DRQ0#				
A9	GBE0_MDI1-	B9	LPC_DRQ1#				
A10	GBE0_MDI1+	B10	LPC_CLK				
A11	GND (FIXED)	B11	GND (FIXED)				
A12	GBE0_MDI0-	B12	PWRBTN#				
A13	GBE0_MDI0+	B13	SMB_CK				
A14	GBE0_CTREF	B14	SMB_DAT				
A15	SUS_S3#	B15	SMB_ALERT#				
A16	SATA0_TX+	B16	SATA1_TX+				
A17	SATA0_TX-	B17	SATA1_TX-				
A18	SUS_S4#	B18	SUS_STAT#				
A19	SATA0_RX+	B19	SATA1_RX+				
A20	SATA0_RX-	B20	SATA1_RX-				
A21	GND (FIXED)	B21	GND (FIXED)				
A22	SATA2_TX+	B22	SATA3_TX+				
A23	SATA2_TX-	B23	SATA3_TX-				
A24	SUS_S5#	B24	PWR_OK				
A25	SATA2_RX+	B25	SATA3_RX+				
A26	SATA2_RX-	B26	SATA3_RX-				
A27	BATLOW#	B27	WDT				
A28	ATA_ACT#	B28	AC_SDIN2				
A29	AC_SYNC	B29	AC_SDIN1				
A30	AC_RST#	B30	AC_SDIN0				
A31	GND (FIXED)	B31	GND (FIXED)				
A32	AC_BITCLK	B32	SPKR				
A33	AC_SDOUT	B33	I2C_CK				
A34	BIOS_DISABLE#	B34	I2C_DAT				
A35	THRMTRIP#	B35	THRM#				
A36	USB6-	B36	USB7-				
A37	USB6+	B37	USB7+				
A38	USB_6_7_OC#	B38	USB_4_5_OC#				
A39	USB4-	B39	USB5-				
A40	USB4+	B40	USB5+				
A41	GND (FIXED)	B41	GND (FIXED)				
A42	USB2-	B42	USB3-				
A43	USB2+	B43	USB3+				
A44	USB_2_3_OC#	B44	USB_0_1_OC#				
A45	USB0-	B45	USB1-				
A46	USB0+	B46	USB1+				
A47	VCC_RTC	B47	EXCD1_PERST#				
A48	EXCD0_PERST#	B48	EXCD1_CPPE#				
A49	EXCD0_CPPE#	B49	SYS_RESET#				
A50	LPC_SERIRQ	B50	CB_RESET#				

A51	GND (FIXED)		B51	GND (FIXED)						
A52	PCIE_TX5+		B52	PCIE_RX5+						
A53	PCIE_TX5-		B53	PCIE_RX5-						
A54	GPI0		B54	GPO1						
A55	PCIE_TX4+		B55	PCIE_RX4+						
A56	PCIE_TX4-		B56	PCIE_RX4-						
A57	GND		B57	GPO2						
A58	PCIE_TX3+		B58	PCIE_RX3+						
A59	PCIE_TX3-		B59	PCIE_RX3-						
A60	GND (FIXED)		B60	GND (FIXED)						
A61	PCIE_TX2+		B61	PCIE_RX2+						
A62	PCIE_TX2-		B62	PCIE_RX2-						
A63	GPI1		B63	GPO3						
A64	PCIE_TX1+		B64	PCIE_RX1+						
A65	PCIE_TX1-		B65	PCIE_RX1-						
A66	GND		B66	WAKE0#						
A67	GPI2		B67	WAKE1#						
A68	PCIE_TX0+		B68	PCIE_RX0+						
A69	PCIE_TX0-		B69	PCIE_RX0-						
A70	GND (FIXED)		B70	GND (FIXED)						
A71	LVDS_A0+		B71	LVDS_B0+						
A72	LVDS_A0-		B72	LVDS_B0-						
A73	LVDS_A1+		B73	LVDS_B1+						
A74	LVDS_A1-		B74	LVDS_B1-						
A75	LVDS_A2+		B75	LVDS_B2+						
A76	LVDS_A2-		B76	LVDS_B2-						
A77	LVDS_VDD_EN		B77	LVDS_B3+						
A78	LVDS_A3+		B78	LVDS_B3-						
A79	LVDS_A3-		B79	LVDS_BKLT_EN						
A80	GND (FIXED)		B80	GND (FIXED)						
A81	LVDS_A_CK+		B81	LVDS_B_CK+						
A82	LVDS_A_CK-		B82	LVDS_B_CK-						
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL						
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY						
A85	GPI3		B85	VCC_5V_SBY						
A86	KBD_RST#		B86	VCC_5V_SBY						
A87	KBD_A20GATE		B87	VCC_5V_SBY						
A88	PCIE0_CK_REF+		B88	RSVD						
A89	PCIE0_CK_REF-		B89	VGA_RED						
A90	GND (FIXED)		B90	GND (FIXED)						
A91	RSVD		B91	VGA_GRN						
A92	RSVD		B92	VGA_BLU						
A93	GPO0		B93	VGA_HSYNC						
A94	RSVD		B94	VGA_VSYNC						
A95	RSVD		B95	VGA_I2C_CK						
A96	GND		B96	VGA_I2C_DAT						
A97	VCC_12V		B97	TV_DAC_A						
A98	VCC_12V		B98	TV_DAC_B						
A99	VCC_12V		B99	TV_DAC_C						
A100	GND (FIXED)		B100	GND (FIXED)						
A101	VCC_12V		B101	VCC_12V						
A102	VCC_12V		B102	VCC_12V						
A103	VCC_12V		B103	VCC_12V						
A104	VCC_12V		B104	VCC_12V						
A105	VCC_12V		B105	VCC_12V						
A106	VCC_12V		B106	VCC_12V						
A107	VCC_12V		B107	VCC_12V						
A108	VCC_12V		B108	VCC_12V						
A109	VCC_12V		B109	VCC_12V						
A110	GND (FIXED)		B110	GND (FIXED)						

Table 4-3: Pin List for Pin-out Type 2

Type 2 includes PCI, IDE, a single GBE, up to 22 general-purpose PCIE lanes (PCIE 0-5 and PCIE 16-31). For most Type 2 implementations, it is expected that PCIE lanes 16-31 are used for graphics. Hence they are designated PEG lanes 0-15 in this table. Modules implementing Pin-out Type 2 **shall** use the pin-out shown in this table. Refer to Table 3-2 for minimum requirements and Table 3-3 for the order in which interfaces **shall** be implemented.

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	IDE_D7	D2	IDE_D5
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	IDE_D6	D3	IDE_D10
A4	GBE0_LINK100#	B4	LPC_AD0	C4	IDE_D3	D4	IDE_D11
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	IDE_D15	D5	IDE_D12
A6	GBE0_MDI2-	B6	LPC_AD2	C6	IDE_D8	D6	IDE_D4
A7	GBE0_MDI2+	B7	LPC_AD3	C7	IDE_D9	D7	IDE_D0
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	IDE_D2	D8	IDE_REQ
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	IDE_D13	D9	IDE_IOW#
A10	GBE0_MDI1+	B10	LPC_CLK	C10	IDE_D1	D10	IDE_ACK#
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	IDE_D14	D12	IDE_IRQ
A13	GBE0_MDI0+	B13	SMB_CK	C13	IDE_IORDY	D13	IDE_A0
A14	GBE0_CTREF	B14	SMB_DAT	C14	IDE_IOR#	D14	IDE_A1
A15	SUS_S3#	B15	SMB_ALERT#	C15	PCI_PME#	D15	IDE_A2
A16	SATA0_TX+	B16	SATA1_TX+	C16	PCI_GNT2#	D16	IDE_CS1#
A17	SATA0_TX-	B17	SATA1_TX-	C17	PCI_REQ2#	D17	IDE_CS3#
A18	SUS_S4#	B18	SUS_STAT#	C18	PCI_GNT1#	D18	IDE_RESET#
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCI_REQ1#	D19	PCI_GNT3#
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCI_GNT0#	D20	PCI_REQ3#
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	C22	PCI_REQ0#	D22	PCI_AD1
A23	SATA2_TX-	B23	SATA3_TX-	C23	PCI_RESET#	D23	PCI_AD3
A24	SUS_S5#	B24	PWR_OK	C24	PCI_AD0	D24	PCI_AD5
A25	SATA2_RX+	B25	SATA3_RX+	C25	PCI_AD2	D25	PCI_AD7
A26	SATA2_RX-	B26	SATA3_RX-	C26	PCI_AD4	D26	PCI_C/BE0#
A27	BATLOW#	B27	WDT	C27	PCI_AD6	D27	PCI_AD9
A28	ATA_ACT#	B28	AC_SDIN2	C28	PCI_AD8	D28	PCI_AD11
A29	AC_SYNC	B29	AC_SDIN1	C29	PCI_AD10	D29	PCI_AD13
A30	AC_RST#	B30	AC_SDIN0	C30	PCI_AD12	D30	PCI_AD15
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	C32	PCI_AD14	D32	PCI_PAR
A33	AC_SDOUT	B33	I2C_CK	C33	PCI_C/BE1#	D33	PCI_SERR#
A34	BIOS_DISABLE#	B34	I2C_DAT	C34	PCI_PERR#	D34	PCI_STOP#
A35	THRMTRIP#	B35	THRM#	C35	PCI_LOCK#	D35	PCI_TRDY#
A36	USB6-	B36	USB7-	C36	PCI_DEVSEL#	D36	PCI_FRAME#
A37	USB6+	B37	USB7+	C37	PCI_IRDY#	D37	PCI_AD16
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	PCI_C/BE2#	D38	PCI_AD18
A39	USB4-	B39	USB5-	C39	PCI_AD17	D39	PCI_AD20
A40	USB4+	B40	USB5+	C40	PCI_AD19	D40	PCI_AD22
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	PCI_AD21	D42	PCI_AD24
A43	USB2+	B43	USB3+	C43	PCI_AD23	D43	PCI_AD26
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	PCI_C/BE3#	D44	PCI_AD28
A45	USB0-	B45	USB1-	C45	PCI_AD25	D45	PCI_AD30
A46	USB0+	B46	USB1+	C46	PCI_AD27	D46	PCI_IRQC#
A47	VCC_RTC	B47	EXCD1_PERST#	C47	PCI_AD29	D47	PCI_IRQD#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	PCI_AD31	D48	PCI_CLKRUN#
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	PCI_IRQA#	D49	PCI_M66EN
A50	LPC_SERIRQ	B50	CB_RESET#	C50	PCI_IRQB#	D50	PCI_CLK

Signal Descriptions

A51	GND (FIXED)		B51	GND (FIXED)		C51	GND (FIXED)		D51	GND (FIXED)
A52	PCIE_TX5+		B52	PCIE_RX5+		C52	PEG_RX0+		D52	PEG_TX0+
A53	PCIE_TX5-		B53	PCIE_RX5-		C53	PEG_RX0-		D53	PEG_TX0-
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	PEG_LANE_RV#
A55	PCIE_TX4+		B55	PCIE_RX4+		C55	PEG_RX1+		D55	PEG_TX1+
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PEG_RX1-		D56	PEG_TX1-
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PEG_RX2+		D58	PEG_TX2+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PEG_RX2-		D59	PEG_TX2-
A60	GND (FIXED)		B60	GND (FIXED)		C60	GND (FIXED)		D60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PEG_RX3+		D61	PEG_TX3+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PEG_RX3-		D62	PEG_TX3-
A63	GPI1		B63	GPO3		C63	RSVD		D63	RSVD
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	RSVD		D64	RSVD
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PEG_RX4+		D65	PEG_TX4+
A66	GND		B66	WAKE0#		C66	PEG_RX4-		D66	PEG_TX4-
A67	GPI2		B67	WAKE1#		C67	RSVD		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PEG_RX5+		D68	PEG_TX5+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PEG_RX5-		D69	PEG_TX5-
A70	GND (FIXED)		B70	GND (FIXED)		C70	GND (FIXED)		D70	GND (FIXED)
A71	LVDS_A0+		B71	LVDS_B0+		C71	PEG_RX6+		D71	PEG_TX6+
A72	LVDS_A0-		B72	LVDS_B0-		C72	PEG_RX6-		D72	PEG_TX6-
A73	LVDS_A1+		B73	LVDS_B1+		C73	SDVO_DATA		D73	SDVO_CLK
A74	LVDS_A1-		B74	LVDS_B1-		C74	PEG_RX7+		D74	PEG_TX7+
A75	LVDS_A2+		B75	LVDS_B2+		C75	PEG_RX7-		D75	PEG_TX7-
A76	LVDS_A2-		B76	LVDS_B2-		C76	GND		D76	GND
A77	LVDS_VDD_EN		B77	LVDS_B3+		C77	RSVD		D77	IDE_CBLID#
A78	LVDS_A3+		B78	LVDS_B3-		C78	PEG_RX8+		D78	PEG_TX8+
A79	LVDS_A3-		B79	LVDS_BKLT_EN		C79	PEG_RX8-		D79	PEG_TX8-
A80	GND (FIXED)		B80	GND (FIXED)		C80	GND (FIXED)		D80	GND (FIXED)
A81	LVDS_A_CK+		B81	LVDS_B_CK+		C81	PEG_RX9+		D81	PEG_TX9+
A82	LVDS_A_CK-		B82	LVDS_B_CK-		C82	PEG_RX9-		D82	PEG_TX9-
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL		C83	RSVD		D83	RSVD
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		C85	PEG_RX10+		D85	PEG_TX10+
A86	KBD_RST#		B86	VCC_5V_SBY		C86	PEG_RX10-		D86	PEG_TX10-
A87	KBD_A20GATE		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE0_CK_REF+		B88	RSVD		C88	PEG_RX11+		D88	PEG_TX11+
A89	PCIE0_CK_REF-		B89	VGA_RED		C89	PEG_RX11-		D89	PEG_TX11-
A90	GND (FIXED)		B90	GND (FIXED)		C90	GND (FIXED)		D90	GND (FIXED)
A91	RSVD		B91	VGA_GRN		C91	PEG_RX12+		D91	PEG_TX12+
A92	RSVD		B92	VGA_BLU		C92	PEG_RX12-		D92	PEG_TX12-
A93	GPO0		B93	VGA_HSYNC		C93	GND		D93	GND
A94	RSVD		B94	VGA_VSYNC		C94	PEG_RX13+		D94	PEG_TX13+
A95	RSVD		B95	VGA_I2C_CK		C95	PEG_RX13-		D95	PEG_TX13-
A96	GND		B96	VGA_I2C_DAT		C96	GND		D96	GND
A97	VCC_12V		B97	TV_DAC_A		C97	RSVD		D97	PEG_ENABLE#
A98	VCC_12V		B98	TV_DAC_B		C98	PEG_RX14+		D98	PEG_TX14+
A99	VCC_12V		B99	TV_DAC_C		C99	PEG_RX14-		D99	PEG_TX14-
A100	GND (FIXED)		B100	GND (FIXED)		C100	GND (FIXED)		D100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V		C101	PEG_RX15+		D101	PEG_TX15+
A102	VCC_12V		B102	VCC_12V		C102	PEG_RX15-		D102	PEG_TX15-
A103	VCC_12V		B103	VCC_12V		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Table 4-4: Pin List for Pin-out Type 3

Differences relative to Type 2 shown in bold. Type 3 reassigns IDE to two additional GBE ports. Modules implementing Pin-out Type 3 **shall** use the pin-out shown in this table. Refer to Table 3-2 for minimum requirements and Table 3-3 for the order in which interfaces **shall** be implemented.

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	**C2**	**GBE1_ACT#**	**D2**	**GBE2_ACT#**
A3	GBE0_MDI3+	B3	LPC_FRAME#	**C3**	**GBE1_MDI3-**	**D3**	**GBE2_MDI3-**
A4	GBE0_LINK100#	B4	LPC_AD0	**C4**	**GBE1_MDI3+**	**D4**	**GBE2_MDI3+**
A5	GBE0_LINK1000#	B5	LPC_AD1	**C5**	**GBE1_LINK100#**	**D5**	**GBE2_LINK100#**
A6	GBE0_MDI2-	B6	LPC_AD2	**C6**	**GBE1_MDI2-**	**D6**	**GBE2_MDI2-**
A7	GBE0_MDI2+	B7	LPC_AD3	**C7**	**GBE1_MDI2+**	**D7**	**GBE2_MDI2+**
A8	GBE0_LINK#	B8	LPC_DRQ0#	**C8**	**GBE1_LINK1000#**	**D8**	**GBE2_LINK1000#**
A9	GBE0_MDI1-	B9	LPC_DRQ1#	**C9**	**GBE1_MDI1-**	**D9**	**GBE2_MDI1-**
A10	GBE0_MDI1+	B10	LPC_CLK	**C10**	**GBE1_MDI1+**	**D10**	**GBE2_MDI1+**
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	**C12**	**GBE1_MDI0-**	**D12**	**GBE2_MDI0-**
A13	GBE0_MDI0+	B13	SMB_CK	**C13**	**GBE1_MDI0+**	**D13**	**GBE2_MDI0+**
A14	GBE0_CTREF	B14	SMB_DAT	**C14**	**GBE1_LINK#**	**D14**	**GBE2_LINK#**
A15	SUS_S3#	B15	SMB_ALERT#	C15	PCI_PME#	**D15**	**GBE2_CTREF**
A16	SATA0_TX+	B16	SATA1_TX+	C16	PCI_GNT2#	**D16**	**RSVD**
A17	SATA0_TX-	B17	SATA1_TX-	C17	PCI_REQ2#	**D17**	**RSVD**
A18	SUS_S4#	B18	SUS_STAT#	C18	PCI_GNT1#	**D18**	**RSVD**
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCI_REQ1#	D19	PCI_GNT3#
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCI_GNT0#	D20	PCI_REQ3#
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	C22	PCI_REQ0#	D22	PCI_AD1
A23	SATA2_TX-	B23	SATA3_TX-	C23	PCI_RESET#	D23	PCI_AD3
A24	SUS_S5#	B24	PWR_OK	C24	PCI_AD0	D24	PCI_AD5
A25	SATA2_RX+	B25	SATA3_RX+	C25	PCI_AD2	D25	PCI_AD7
A26	SATA2_RX-	B26	SATA3_RX-	C26	PCI_AD4	D26	PCI_C/BE0#
A27	BATLOW#	B27	WDT	C27	PCI_AD6	D27	PCI_AD9
A28	ATA_ACT#	B28	AC_SDIN2	C28	PCI_AD8	D28	PCI_AD11
A29	AC_SYNC	B29	AC_SDIN1	C29	PCI_AD10	D29	PCI_AD13
A30	AC_RST#	B30	AC_SDIN0	C30	PCI_AD12	D30	PCI_AD15
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	C32	PCI_AD14	D32	PCI_PAR
A33	AC_SDOUT	B33	I2C_CK	C33	PCI_C/BE1#	D33	PCI_SERR#
A34	BIOS_DISABLE#	B34	I2C_DAT	C34	PCI_PERR#	D34	PCI_STOP#
A35	THRMTRIP#	B35	THRM#	C35	PCI_LOCK#	D35	PCI_TRDY#
A36	USB6-	B36	USB7-	C36	PCI_DEVSEL#	D36	PCI_FRAME#
A37	USB6+	B37	USB7+	C37	PCI_IRDY#	D37	PCI_AD16
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	PCI_C/BE2#	D38	PCI_AD18
A39	USB4-	B39	USB5-	C39	PCI_AD17	D39	PCI_AD20
A40	USB4+	B40	USB5+	C40	PCI_AD19	D40	PCI_AD22
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	PCI_AD21	D42	PCI_AD24
A43	USB2+	B43	USB3+	C43	PCI_AD23	D43	PCI_AD26
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	PCI_C/BE3#	D44	PCI_AD28
A45	USB0-	B45	USB1-	C45	PCI_AD25	D45	PCI_AD30
A46	USB0+	B46	USB1+	C46	PCI_AD27	D46	PCI_IRQC#
A47	VCC_RTC	B47	EXCD1_PERST#	C47	PCI_AD29	D47	PCI_IRQD#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	PCI_AD31	D48	PCI_CLKRUN#
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	PCI_IRQA#	D49	PCI_M66EN
A50	LPC_SERIRQ	B50	CB_RESET#	C50	PCI_IRQB#	D50	PCI_CLK

A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PEG_RX0+	D52	PEG_TX0+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	PEG_LANE_RV#
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PEG_RX1+	D55	PEG_TX1+
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PEG_RX2+	D58	PEG_TX2+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PEG_RX2-	D59	PEG_TX2-
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PEG_RX3+	D61	PEG_TX3+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PEG_RX3-	D62	PEG_TX3-
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PEG_RX4+	D65	PEG_TX4+
A66	GND	B66	WAKE0#	C66	PEG_RX4-	D66	PEG_TX4-
A67	GPI2	B67	WAKE1#	C67	RSVD	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PEG_RX5+	D68	PEG_TX5+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PEG_RX5-	D69	PEG_TX5-
A70	GND (FIXED)	B70	GND (FIXED)	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71	PEG_RX6+	D71	PEG_TX6+
A72	LVDS_A0-	B72	LVDS_B0-	C72	PEG_RX6-	D72	PEG_TX6-
A73	LVDS_A1+	B73	LVDS_B1+	C73	SDVO_DATA	D73	SDVO_CLK
A74	LVDS_A1-	B74	LVDS_B1-	C74	PEG_RX7+	D74	PEG_TX7+
A75	LVDS_A2+	B75	LVDS_B2+	C75	PEG_RX7-	D75	PEG_TX7-
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD	**D77**	**RSVD**
A78	LVDS_A3+	B78	LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	RSVD	D83	RSVD
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	KBD_RST#	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	KBD_A20GATE	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE0_CK_REF+	B88	RSVD	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE0_CK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	RSVD	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	RSVD	B92	VGA_BLU	C92	PEG_RX12-	D92	PEG_TX12-
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	RSVD	B94	VGA_VSYNC	C94	PEG_RX13+	D94	PEG_TX13+
A95	RSVD	B95	VGA_I2C_CK	C95	PEG_RX13-	D95	PEG_TX13-
A96	GND	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	VCC_12V	B97	TV_DAC_A	C97	RSVD	D97	PEG_ENABLE#
A98	VCC_12V	B98	TV_DAC_B	C98	PEG_RX14+	D98	PEG_TX14+
A99	VCC_12V	B99	TV_DAC_C	C99	PEG_RX14-	D99	PEG_TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	VCC_12V	B101	VCC_12V	C101	PEG_RX15+	D101	PEG_TX15+
A102	VCC_12V	B102	VCC_12V	C102	PEG_RX15-	D102	PEG_TX15-
A103	VCC_12V	B103	VCC_12V	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

Table 4-5: Pin List for Pin-out Type 4

Differences relative to Type 2 shown in bold. Type 4 reassigns PCI to create 10 additional PCIE lanes. PEG lanes 0-15 are renamed PCIE lanes 16-31. These lanes **may** be used as PEG lanes 0-15 or as general purpose PCIE lanes 16-31. Modules implementing Pin-out Type 4 **shall** use the pin-out shown in this table. Refer to Table 3-2 for minimum requirements and Table 3-3 for the order in which interfaces **shall** be implemented.

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	IDE_D7	D2	IDE_D5
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	IDE_D6	D3	IDE_D10
A4	GBE0_LINK100#	B4	LPC_AD0	C4	IDE_D3	D4	IDE_D11
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	IDE_D15	D5	IDE_D12
A6	GBE0_MDI2-	B6	LPC_AD2	C6	IDE_D8	D6	IDE_D4
A7	GBE0_MDI2+	B7	LPC_AD3	C7	IDE_D9	D7	IDE_D0
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	IDE_D2	D8	IDE_REQ
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	IDE_D13	D9	IDE_IOW#
A10	GBE0_MDI1+	B10	LPC_CLK	C10	IDE_D1	D10	IDE_ACK#
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	IDE_D14	D12	IDE_IRQ
A13	GBE0_MDI0+	B13	SMB_CK	C13	IDE_IORDY	D13	IDE_A0
A14	GBE0_CTREF	B14	SMB_DAT	C14	IDE_IOR#	D14	IDE_A1
A15	SUS_S3#	B15	SMB_ALERT#	**C15**	**RSVD**	D15	IDE_A2
A16	SATA0_TX+	B16	SATA1_TX+	**C16**	**RSVD**	D16	IDE_CS1#
A17	SATA0_TX-	B17	SATA1_TX-	**C17**	**RSVD**	D17	IDE_CS3#
A18	SUS_S4#	B18	SUS_STAT#	**C18**	**RSVD**	D18	IDE_RESET#
A19	SATA0_RX+	B19	SATA1_RX+	**C19**	**PCIE_RX6+**	**D19**	**PCIE_TX6+**
A20	SATA0_RX-	B20	SATA1_RX-	**C20**	**PCIE_RX6-**	**D20**	**PCIE_TX6-**
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	**C22**	**PCIE_RX7+**	**D22**	**PCIE_TX7+**
A23	SATA2_TX-	B23	SATA3_TX-	**C23**	**PCIE_RX7-**	**D23**	**PCIE_TX7-**
A24	SUS_S5#	B24	PWR_OK	**C24**	**RSVD**	**D24**	**RSVD**
A25	SATA2_RX+	B25	SATA3_RX+	**C25**	**RSVD**	**D25**	**RSVD**
A26	SATA2_RX-	B26	SATA3_RX-	**C26**	**PCIE_RX8+**	**D26**	**PCIE_TX8+**
A27	BATLOW#	B27	WDT	**C27**	**PCIE_RX8-**	**D27**	**PCIE_TX8-**
A28	ATA_ACT#	B28	AC_SDIN2	**C28**	**RSVD**	**D28**	**RSVD**
A29	AC_SYNC	B29	AC_SDIN1	**C29**	**PCIE_RX9+**	**D29**	**PCIE_TX9+**
A30	AC_RST#	B30	AC_SDIN0	**C30**	**PCIE_RX9-**	**D30**	**PCIE_TX9-**
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	**C32**	**PCIE_RX10+**	**D32**	**PCIE_TX10+**
A33	AC_SDOUT	B33	I2C_CK	**C33**	**PCIE_RX10-**	**D33**	**PCIE_TX10-**
A34	BIOS_DISABLE#	B34	I2C_DAT	**C34**	**RSVD**	**D34**	**RSVD**
A35	THRMTRIP#	B35	THRM#	**C35**	**RSVD**	**D35**	**RSVD**
A36	USB6-	B36	USB7-	**C36**	**PCIE_RX11+**	**D36**	**PCIE_TX11+**
A37	USB6+	B37	USB7+	**C37**	**PCIE_RX11-**	**D37**	**PCIE_TX11-**
A38	USB_6_7_OC#	B38	USB_4_5_OC#	**C38**	**RSVD**	**D38**	**RSVD**
A39	USB4-	B39	USB5-	**C39**	**PCIE_RX12+**	**D39**	**PCIE_TX12+**
A40	USB4+	B40	USB5+	**C40**	**PCIE_RX12-**	**D40**	**PCIE_TX12-**
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	**C42**	**PCIE_RX13+**	**D42**	**PCIE_TX13+**
A43	USB2+	B43	USB3+	**C43**	**PCIE_RX13-**	**D43**	**PCIE_TX13-**
A44	USB_2_3_OC#	B44	USB_0_1_OC#	**C44**	**RSVD**	**D44**	**RSVD**
A45	USB0-	B45	USB1-	**C45**	**RSVD**	**D45**	**RSVD**
A46	USB0+	B46	USB1+	**C46**	**PCIE_RX14+**	**D46**	**PCIE_TX14+**
A47	VCC_RTC	B47	EXCD1_PERST#	**C47**	**PCIE_RX14-**	**D47**	**PCIE_TX14-**
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	**C48**	**RSVD**	**D48**	**RSVD**
A49	EXCD0_CPPE#	B49	SYS_RESET#	**C49**	**PCIE_RX15+**	**D49**	**PCIE_TX15+**
A50	LPC_SERIRQ	B50	CB_RESET#	**C50**	**PCIE_RX15-**	**D50**	**PCIE_TX15-**

A51	GND (FIXED)		B51	GND (FIXED)		C51	GND (FIXED)		D51	GND (FIXED)
A52	PCIE_TX5+		B52	PCIE_RX5+		**C52**	**PCIE_RX16+**		**D52**	**PCIE_TX16+**
A53	PCIE_TX5-		B53	PCIE_RX5-		**C53**	**PCIE_RX16-**		**D53**	**PCIE_TX16-**
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	PEG_LANE_RV#
A55	PCIE_TX4+		B55	PCIE_RX4+		**C55**	**PCIE_RX17+**		**D55**	**PCIE_TX17+**
A56	PCIE_TX4-		B56	PCIE_RX4-		**C56**	**PCIE_RX17-**		**D56**	**PCIE_TX17-**
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		**C58**	**PCIE_RX18+**		**D58**	**PCIE_TX18+**
A59	PCIE_TX3-		B59	PCIE_RX3-		**C59**	**PCIE_RX18-**		**D59**	**PCIE_TX18-**
A60	GND (FIXED)		B60	GND (FIXED)		C60	GND (FIXED)		D60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+		**C61**	**PCIE_RX19+**		**D61**	**PCIE_TX19+**
A62	PCIE_TX2-		B62	PCIE_RX2-		**C62**	**PCIE_RX19-**		**D62**	**PCIE_TX19-**
A63	GPI1		B63	GPO3		C63	RSVD		D63	RSVD
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	RSVD		D64	RSVD
A65	PCIE_TX1-		B65	PCIE_RX1-		**C65**	**PCIE_RX20+**		**D65**	**PCIE_TX20+**
A66	GND		B66	WAKE0#		**C66**	**PCIE_RX20-**		**D66**	**PCIE_TX20-**
A67	GPI2		B67	WAKE1#		C67	RSVD		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		**C68**	**PCIE_RX21+**		**D68**	**PCIE_TX21+**
A69	PCIE_TX0-		B69	PCIE_RX0-		**C69**	**PCIE_RX21-**		**D69**	**PCIE_TX21-**
A70	GND (FIXED)		B70	GND (FIXED)		C70	GND (FIXED)		D70	GND (FIXED)
A71	LVDS_A0+		B71	LVDS_B0+		**C71**	**PCIE_RX22+**		**D71**	**PCIE_TX22+**
A72	LVDS_A0-		B72	LVDS_B0-		**C72**	**PCIE_RX22-**		**D72**	**PCIE_TX22-**
A73	LVDS_A1+		B73	LVDS_B1+		C73	SDVO_DATA		D73	SDVO_CLK
A74	LVDS_A1-		B74	LVDS_B1-		**C74**	**PCIE_RX23+**		**D74**	**PCIE_TX23+**
A75	LVDS_A2+		B75	LVDS_B2+		**C75**	**PCIE_RX23-**		**D75**	**PCIE_TX23-**
A76	LVDS_A2-		B76	LVDS_B2-		C76	GND		D76	GND
A77	LVDS_VDD_EN		B77	LVDS_B3+		C77	RSVD		D77	IDE_CBLID#
A78	LVDS_A3+		B78	LVDS_B3-		**C78**	**PCIE_RX24+**		**D78**	**PCIE_TX24+**
A79	LVDS_A3-		B79	LVDS_BKLT_EN		**C79**	**PCIE_RX24-**		**D79**	**PCIE_TX24-**
A80	GND (FIXED)		B80	GND (FIXED)		C80	GND (FIXED)		D80	GND (FIXED)
A81	LVDS_A_CK+		B81	LVDS_B_CK+		**C81**	**PCIE_RX25+**		**D81**	**PCIE_TX25+**
A82	LVDS_A_CK-		B82	LVDS_B_CK-		**C82**	**PCIE_RX25-**		**D82**	**PCIE_TX25-**
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL		C83	RSVD		D83	RSVD
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		**C85**	**PCIE_RX26+**		**D85**	**PCIE_TX26+**
A86	KBD_RST#		B86	VCC_5V_SBY		**C86**	**PCIE_RX26-**		**D86**	**PCIE_TX26-**
A87	KBD_A20GATE		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE0_CK_REF+		B88	RSVD		**C88**	**PCIE_RX27+**		**D88**	**PCIE_TX27+**
A89	PCIE0_CK_REF-		B89	VGA_RED		**C89**	**PCIE_RX27-**		**D89**	**PCIE_TX27-**
A90	GND (FIXED)		B90	GND (FIXED)		C90	GND (FIXED)		D90	GND (FIXED)
A91	RSVD		B91	VGA_GRN		**C91**	**PCIE_RX28+**		**D91**	**PCIE_TX28+**
A92	RSVD		B92	VGA_BLU		**C92**	**PCIE_RX28-**		**D92**	**PCIE_TX28-**
A93	GPO0		B93	VGA_HSYNC		C93	GND		D93	GND
A94	RSVD		B94	VGA_VSYNC		**C94**	**PCIE_RX29+**		**D94**	**PCIE_TX29+**
A95	RSVD		B95	VGA_I2C_CK		**C95**	**PCIE_RX29-**		**D95**	**PCIE_TX29-**
A96	GND		B96	VGA_I2C_DAT		C96	GND		D96	GND
A97	VCC_12V		B97	TV_DAC_A		C97	RSVD		D97	PEG_ENABLE#
A98	VCC_12V		B98	TV_DAC_B		**C98**	**PCIE_RX30+**		**D98**	**PCIE_TX30+**
A99	VCC_12V		B99	TV_DAC_C		**C99**	**PCIE_RX30-**		**D99**	**PCIE_TX30-**
A100	GND (FIXED)		B100	GND (FIXED)		C100	GND (FIXED)		D100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V		C101	**PCIE_RX31+**		**D101**	**PCIE_TX31+**
A102	VCC_12V		B102	VCC_12V		C102	**PCIE_RX31-**		**D102**	**PCIE_TX31-**
A103	VCC_12V		B103	VCC_12V		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Table 4-6: Pin List for Pin-out Type 5

Differences relative to Type 2 shown in bold. Type 5 reassigns PCI to 10 additional PCIE lanes and IDE to 2 additional GBE ports. PEG lanes 0-15 are renamed PCIE lanes 16-31. These lanes **may** be used as PEG lanes 0-15 or as general purpose PCIE lanes 16-31. Modules implementing Pin-out Type 5 **shall** use the pin-out shown in this table. Refer to Table 3-2 for minimum requirements and Table 3-3 for the order in which interfaces **shall** be implemented.

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	**C2**	**GBE1_ACT#**	**D2**	**GBE2_ACT#**
A3	GBE0_MDI3+	B3	LPC_FRAME#	**C3**	**GBE1_MDI3-**	**D3**	**GBE2_MDI3-**
A4	GBE0_LINK100#	B4	LPC_AD0	**C4**	**GBE1_MDI3+**	**D4**	**GBE2_MDI3+**
A5	GBE0_LINK1000#	B5	LPC_AD1	**C5**	**GBE1_LINK100#**	**D5**	**GBE2_LINK100#**
A6	GBE0_MDI2-	B6	LPC_AD2	**C6**	**GBE1_MDI2-**	**D6**	**GBE2_MDI2-**
A7	GBE0_MDI2+	B7	LPC_AD3	**C7**	**GBE1_MDI2+**	**D7**	**GBE2_MDI2+**
A8	GBE0_LINK#	B8	LPC_DRQ0#	**C8**	**GBE1_LINK1000#**	**D8**	**GBE2_LINK1000#**
A9	GBE0_MDI1-	B9	LPC_DRQ1#	**C9**	**GBE1_MDI1-**	**D9**	**GBE2_MDI1-**
A10	GBE0_MDI1+	B10	LPC_CLK	**C10**	**GBE1_MDI1+**	**D10**	**GBE2_MDI1+**
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	**C12**	**GBE1_MDI0-**	**D12**	**GBE2_MDI0-**
A13	GBE0_MDI0+	B13	SMB_CK	**C13**	**GBE1_MDI0+**	**D13**	**GBE2_MDI0+**
A14	GBE0_CTREF	B14	SMB_DAT	**C14**	**GBE1_LINK#**	**D14**	**GBE2_LINK#**
A15	SUS_S3#	B15	SMB_ALERT#	**C15**	**RSVD**	**D15**	**GBE2_CTREF**
A16	SATA0_TX+	B16	SATA1_TX+	**C16**	**RSVD**	**D16**	**RSVD**
A17	SATA0_TX-	B17	SATA1_TX-	**C17**	**RSVD**	**D17**	**RSVD**
A18	SUS_S4#	B18	SUS_STAT#	**C18**	**RSVD**	**D18**	**RSVD**
A19	SATA0_RX+	B19	SATA1_RX+	**C19**	**PCIE_RX6+**	**D19**	**PCIE_TX6+**
A20	SATA0_RX-	B20	SATA1_RX-	**C20**	**PCIE_RX6-**	**D20**	**PCIE_TX6-**
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	**C22**	**PCIE_RX7+**	**D22**	**PCIE_TX7+**
A23	SATA2_TX-	B23	SATA3_TX-	**C23**	**PCIE_RX7-**	**D23**	**PCIE_TX7-**
A24	SUS_S5#	B24	PWR_OK	**C24**	**RSVD**	**D24**	**RSVD**
A25	SATA2_RX+	B25	SATA3_RX+	**C25**	**RSVD**	**D25**	**RSVD**
A26	SATA2_RX-	B26	SATA3_RX-	**C26**	**PCIE_RX8+**	**D26**	**PCIE_TX8+**
A27	BATLOW#	B27	WDT	**C27**	**PCIE_RX8-**	**D27**	**PCIE_TX8-**
A28	ATA_ACT#	B28	AC_SDIN2	**C28**	**RSVD**	**D28**	**RSVD**
A29	AC_SYNC	B29	AC_SDIN1	**C29**	**PCIE_RX9+**	**D29**	**PCIE_TX9+**
A30	AC_RST#	B30	AC_SDIN0	**C30**	**PCIE_RX9-**	**D30**	**PCIE_TX9-**
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	**C32**	**PCIE_RX10+**	**D32**	**PCIE_TX10+**
A33	AC_SDOUT	B33	I2C_CK	**C33**	**PCIE_RX10-**	**D33**	**PCIE_TX10-**
A34	BIOS_DISABLE#	B34	I2C_DAT	**C34**	**RSVD**	**D34**	**RSVD**
A35	THRMTRIP#	B35	THRM#	**C35**	**RSVD**	**D35**	**RSVD**
A36	USB6-	B36	USB7-	**C36**	**PCIE_RX11+**	**D36**	**PCIE_TX11+**
A37	USB6+	B37	USB7+	**C37**	**PCIE_RX11-**	**D37**	**PCIE_TX11-**
A38	USB_6_7_OC#	B38	USB_4_5_OC#	**C38**	**RSVD**	**D38**	**RSVD**
A39	USB4-	B39	USB5-	**C39**	**PCIE_RX12+**	**D39**	**PCIE_TX12+**
A40	USB4+	B40	USB5+	**C40**	**PCIE_RX12-**	**D40**	**PCIE_TX12-**
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	**C42**	**PCIE_RX13+**	**D42**	**PCIE_TX13+**
A43	USB2+	B43	USB3+	**C43**	**PCIE_RX13-**	**D43**	**PCIE_TX13-**
A44	USB_2_3_OC#	B44	USB_0_1_OC#	**C44**	**RSVD**	**D44**	**RSVD**
A45	USB0-	B45	USB1-	**C45**	**RSVD**	**D45**	**RSVD**
A46	USB0+	B46	USB1+	**C46**	**PCIE_RX14+**	**D46**	**PCIE_TX14+**
A47	VCC_RTC	B47	EXCD1_PERST#	**C47**	**PCIE_RX14-**	**D47**	**PCIE_TX14-**
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	**C48**	**RSVD**	**D48**	**RSVD**
A49	EXCD0_CPPE#	B49	SYS_RESET#	**C49**	**PCIE_RX15+**	**D49**	**PCIE_TX15+**
A50	LPC_SERIRQ	B50	CB_RESET#	**C50**	**PCIE_RX15-**	**D50**	**PCIE_TX15-**

A51	GND (FIXED)		B51	GND (FIXED)		C51	GND (FIXED)		D51	GND (FIXED)
A52	PCIE_TX5+		B52	PCIE_RX5+		**C52**	**PCIE_RX16+**		**D52**	**PCIE_TX16+**
A53	PCIE_TX5-		B53	PCIE_RX5-		**C53**	**PCIE_RX16-**		**D53**	**PCIE_TX16-**
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	PEG_LANE_RV#
A55	PCIE_TX4+		B55	PCIE_RX4+		**C55**	**PCIE_RX17+**		**D55**	**PCIE_TX17+**
A56	PCIE_TX4-		B56	PCIE_RX4-		**C56**	**PCIE_RX17-**		**D56**	**PCIE_TX17-**
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		**C58**	**PCIE_RX18+**		**D58**	**PCIE_TX18+**
A59	PCIE_TX3-		B59	PCIE_RX3-		**C59**	**PCIE_RX18-**		**D59**	**PCIE_TX18-**
A60	GND (FIXED)		B60	GND (FIXED)		C60	GND (FIXED)		D60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+		**C61**	**PCIE_RX19+**		**D61**	**PCIE_TX19+**
A62	PCIE_TX2-		B62	PCIE_RX2-		**C62**	**PCIE_RX19-**		**D62**	**PCIE_TX19-**
A63	GPI1		B63	GPO3		C63	RSVD		D63	RSVD
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	RSVD		D64	RSVD
A65	PCIE_TX1-		B65	PCIE_RX1-		**C65**	**PCIE_RX20+**		**D65**	**PCIE_TX20+**
A66	GND		B66	WAKE0#		**C66**	**PCIE_RX20-**		**D66**	**PCIE_TX20-**
A67	GPI2		B67	WAKE1#		C67	RSVD		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		**C68**	**PCIE_RX21+**		**D68**	**PCIE_TX21+**
A69	PCIE_TX0-		B69	PCIE_RX0-		**C69**	**PCIE_RX21-**		**D69**	**PCIE_TX21-**
A70	GND (FIXED)		B70	GND (FIXED)		C70	GND (FIXED)		D70	GND (FIXED)
A71	LVDS_A0+		B71	LVDS_B0+		**C71**	**PCIE_RX22+**		**D71**	**PCIE_TX22+**
A72	LVDS_A0-		B72	LVDS_B0-		**C72**	**PCIE_RX22-**		**D72**	**PCIE_TX22-**
A73	LVDS_A1+		B73	LVDS_B1+		C73	SDVO_DATA		D73	SDVO_CLK
A74	LVDS_A1-		B74	LVDS_B1-		**C74**	**PCIE_RX23+**		**D74**	**PCIE_TX23+**
A75	LVDS_A2+		B75	LVDS_B2+		**C75**	**PCIE_RX23-**		**D75**	**PCIE_TX23-**
A76	LVDS_A2-		B76	LVDS_B2-		C76	GND		D76	GND
A77	LVDS_VDD_EN		B77	LVDS_B3+		C77	RSVD		**D77**	**RSVD**
A78	LVDS_A3+		B78	LVDS_B3-		**C78**	**PCIE_RX24+**		**D78**	**PCIE_TX24+**
A79	LVDS_A3-		B79	LVDS_BKLT_EN		**C79**	**PCIE_RX24-**		**D79**	**PCIE_TX24-**
A80	GND (FIXED)		B80	GND (FIXED)		C80	GND (FIXED)		D80	GND (FIXED)
A81	LVDS_A_CK+		B81	LVDS_B_CK+		**C81**	**PCIE_RX25+**		**D81**	**PCIE_TX25+**
A82	LVDS_A_CK-		B82	LVDS_B_CK-		**C82**	**PCIE_RX25-**		**D82**	**PCIE_TX25-**
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL		C83	RSVD		D83	RSVD
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		**C85**	**PCIE_RX26+**		**D85**	**PCIE_TX26+**
A86	KBD_RST#		B86	VCC_5V_SBY		**C86**	**PCIE_RX26-**		**D86**	**PCIE_TX26-**
A87	KBD_A20GATE		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE0_CK_REF+		B88	RSVD		**C88**	**PCIE_RX27+**		**D88**	**PCIE_TX27+**
A89	PCIE0_CK_REF-		B89	VGA_RED		**C89**	**PCIE_RX27-**		**D89**	**PCIE_TX27-**
A90	GND (FIXED)		B90	GND (FIXED)		C90	GND (FIXED)		D90	GND (FIXED)
A91	RSVD		B91	VGA_GRN		**C91**	**PCIE_RX28+**		**D91**	**PCIE_TX28+**
A92	RSVD		B92	VGA_BLU		**C92**	**PCIE_RX28-**		**D92**	**PCIE_TX28-**
A93	GPO0		B93	VGA_HSYNC		C93	GND		D93	GND
A94	RSVD		B94	VGA_VSYNC		**C94**	**PCIE_RX29+**		**D94**	**PCIE_TX29+**
A95	RSVD		B95	VGA_I2C_CK		**C95**	**PCIE_RX29-**		**D95**	**PCIE_TX29-**
A96	GND		B96	VGA_I2C_DAT		C96	GND		D96	GND
A97	VCC_12V		B97	TV_DAC_A		C97	RSVD		D97	PEG_ENABLE#
A98	VCC_12V		B98	TV_DAC_B		**C98**	**PCIE_RX30+**		**D98**	**PCIE_TX30+**
A99	VCC_12V		B99	TV_DAC_C		**C99**	**PCIE_RX30-**		**D99**	**PCIE_TX30-**
A100	GND (FIXED)		B100	GND (FIXED)		C100	GND (FIXED)		D100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V		C101	**PCIE_RX31+**		**D101**	**PCIE_TX31+**
A102	VCC_12V		B102	VCC_12V		C102	**PCIE_RX31-**		**D102**	**PCIE_TX31-**
A103	VCC_12V		B103	VCC_12V		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

5 Module and Carrier Board Implementation Specifications

5.1 PCI Express Link Configuration Definitions

Lane: a “lane” or “PCI Express lane” is a set of 4 pins on the ETXexpress connector that can be used for a single PCI Express transmit pair and a single receive pair. Clocking information is embedded into the data stream.

Link: a “link” or “PCI Express link” is a group of PCI Express lanes between two PCI Express agents. Allowable link widths are x1, x2, x4, x8, x16 and x32. An x1 link utilizes 1 lane; a x2 link 2 lanes, etc. The link bandwidth scales up proportionally with the link width.

Link Configuration: the ETXexpress connector allows up to 32 PCI Express lanes to be used. The count varies with the module Pin-out Type. Chipsets used on ETXexpress modules have a variety of PCI Express lane and link capabilities. On some chipsets, the PCI Express lanes can be grouped into various links under software control; on other chipsets, the PCI Express links are of a fixed width. The mapping of the chipset PCI Express lanes to the ETXexpress lanes and the grouping of the lanes into links is referred to as “link configuration.”

Bucket: a “bucket” is a group of 8 PCI Express lanes on the ETXexpress connector. The 32 PCI Express lanes on the ETXexpress connector are conceptually divided into 4 buckets to facilitate a description of how the available PCI Express lanes **should** be assigned to ETXexpress connector pins. The “bucket” terminology is only a vehicle to facilitate the description of an orderly mapping of chipset PCI Express lanes to ETXexpress connector PCI Express lanes. A bucket is not a link.

5.2 PCI Express Link Configuration Guidelines

The ETXexpress connector PCI Express lanes are conceptually divided into four "buckets," labeled B1, B2, B3, and B4. The buckets **shall** be filled according to the following rules:

- The fill starts from the lowest lane number in a bucket and proceeds upwards.
- The largest links go into the lower lane numbers in a bucket.
- Links that are 16 lanes wide **shall** span buckets B3 and B4 or buckets B1 and B2.
- PCI Express Graphics (PEG) link(s) **shall** use B3 and B4 for the first link and **shall** use B1 and B2 for a 2nd link.
- Links that span more than one bucket **shall** start in the bucket with the lowest lane number.

Table 5-1: PCI Express Lane Numbers and Bucket Groupings

ETXexpress Pin Label	Lane Number	Availability By Module Pin-out Type	Bucket Reference
PCIE 31	31	Module Pin-out Types 2,3,4,5 (PCI Express Graphics) Module Pin-out Types 2,3,4,5 (PCI Express, general I/O)	Bucket B4
PCIE 30	30		
PCIE 29	29		
PCIE 28	28		
PCIE 27	27		
PCIE 26	26		
PCIE 25	25		
PCIE 24	24		
PCIE 23	23		Bucket B3
PCIE 22	22		
PCIE 21	21		
PCIE 20	20		
PCIE 19	19		
PCIE 18	18		
PCIE 17	17		
PCIE 16	16		
PCIE 15	15	Module Pin-out Type 4,5	Bucket B2
PCIE 14	14		
PCIE 13	13		
PCIE 12	12		
PCIE 11	11		
PCIE 10	10		
PCIE 9	9		
PCIE 8	8		
PCIE 7	7		Bucket B1
PCIE 6	6		
PCIE 5	5	Module Pin-out Types 1,2,3,4,5	
PCIE 4	4		
PCIE 3	3		
PCIE 2	2		
PCIE 1	1		
PCIE 0	0		

While many permutations are possible, the set of tables below indicate the preferred mappings of chipset PCI Express lanes and links to ETXexpress connector lanes and links.

On most module designs, a portion of available ETXexpress PCI Express lanes are used.

Table 5-2: Module Pin-out Type 1 — Preferred PCI Express Lane Groupings

COM Express Pin Label	Lane	Bucket Reference	Preferred Link Configurations							
PCIE 31	31									
PCIE 30	30									
PCIE 29	29									
PCIE 28	28	B4								
PCIE 27	27									
PCIE 26	26									
PCIE 25	25									
PCIE 24	24									
PCIE 23	23									
PCIE 22	22									
PCIE 21	21									
PCIE 20	20	B3								
PCIE 19	19									
PCIE 18	18									
PCIE 17	17									
PCIE 16	16									
PCIE 15	15									
PCIE 14	14									
PCIE 13	13									
PCIE 12	12	B2								
PCIE 11	11									
PCIE 10	10									
PCIE 9	9									
PCIE 8	8									
PCIE 7	7									
PCIE 6	6									
PCIE 5	5								X1	X1
PCIE 4	4						X1	X1	X1	X1
PCIE 3	3				X1		X1		X1	
PCIE 2	2	B1		X1	X1	X4	X1	X4	X1	X4
PCIE 1	1		X1	X1	X1		X1		X1	
PCIE 0	0		X1	X1	X1		X1		X1	

Note: Grey shaded lanes are not available in Pin-out Type 1.

Table 5-3: Module Pin-out Types 2 and 3 — Preferred Lane Groupings: Bucket B1

COM Express Pin Label	Lane	Bucket Reference	Preferred Link Configurations							
PCIE 31	31	B4	PEG	PEG	PEG	PEG	PEG	PEG	PEG	PEG
PCIE 30	30									
PCIE 29	29									
PCIE 28	28									
PCIE 27	27									
PCIE 26	26									
PCIE 25	25									
PCIE 24	24									
PCIE 23	23	B3								
PCIE 22	22									
PCIE 21	21									
PCIE 20	20									
PCIE 19	19									
PCIE 18	18									
PCIE 17	17									
PCIE 16	16									
PCIE 15	15	B2								
PCIE 14	14									
PCIE 13	13									
PCIE 12	12									
PCIE 11	11									
PCIE 10	10									
PCIE 9	9									
PCIE 8	8									
PCIE 7	7									
PCIE 6	6									
PCIE 5	5	B1							X1	X1
PCIE 4	4						X1	X1	X1	X1
PCIE 3	3				X1	X4	X1	X4	X1	X4
PCIE 2	2			X1	X1		X1		X1	
PCIE 1	1		X1	X1	X1		X1		X1	
PCIE 0	0		X1	X1	X1		X1		X1	

Notes:

1) Grey shaded lanes are not available in Pin-out Types 2 and 3.

2) If upper lanes (buckets B3 and B4) are not used for PCI Express Graphics (PEG), then lanes mapped into buckets B3 and B4 **should** be grouped per Table 5-4.

Table 5-4: Module Pin-out Types 2 and 3 — Preferred Lane Groupings: Buckets B3 and B4

COM Express Pin Label	PCI Express Lane	Bucket Reference	Preferred Link Configurations			
PCIE 31	31	B4	X4	X4	X8	X16 (PEG)
PCIE 30	30					
PCIE 29	29					
PCIE 28	28					
PCIE 27	27		X4	X4		
PCIE 26	26					
PCIE 25	25					
PCIE 24	24					
PCIE 23	23	B3	X4	X8	X8	
PCIE 22	22					
PCIE 21	21					
PCIE 20	20					
PCIE 19	19		X4			
PCIE 18	18					
PCIE 17	17					
PCIE 16	16					
PCIE 15	15	B2				
PCIE 14	14					
PCIE 13	13					
PCIE 12	12					
PCIE 11	11					
PCIE 10	10					
PCIE 9	9					
PCIE 8	8					
PCIE 7	7					
PCIE 6	6					
PCIE 5	5	B1	See bucket B1 in Table 5-3			
PCIE 4	4					
PCIE 3	3					
PCIE 2	2					
PCIE 1	1					
PCIE 0	0					

Notes:

1) Grey shaded lanes are not available in Pin-out Types 2 and 3.

2) Bucket B1 groupings for Pin-out Types 2 and 3 covered in Table 5-3.

3) X16 link **may** be used for PCI Express Graphics (PEG) or for general purpose I/O.

Table 5-5: Module Pin-out Types 4 and 5 — Preferred PCI Express Lane Groupings

COM Express Pin Label	Lane	Bucket Reference	Preferred Link Configurations								
PCIE 31	31	B4	X4	X4	X4	X4	X4	X8	X8	X16 (PEG)	X32
PCIE 30	30										
PCIE 29	29										
PCIE 28	28										
PCIE 27	27		X4	X4	X4	X4	X4				
PCIE 26	26										
PCIE 25	25										
PCIE 24	24										
PCIE 23	23	B3	X4	X4	X4	X8	X8	X8	X8		
PCIE 22	22										
PCIE 21	21										
PCIE 20	20										
PCIE 19	19		X4	X4	X4						
PCIE 18	18										
PCIE 17	17										
PCIE 16	16										
PCIE 15	15	B2	X4	X4	X8	X8	X8	X8	X16	X16	
PCIE 14	14										
PCIE 13	13										
PCIE 12	12										
PCIE 11	11		X4	X4							
PCIE 10	10										
PCIE 9	9										
PCIE 8	8										
PCIE 7	7	B1	X4	X8	X8	X8	X8	X8			
PCIE 6	6										
PCIE 5	5										
PCIE 4	4										
PCIE 3	3		X4								
PCIE 2	2										
PCIE 1	1										
PCIE 0	0										

5.3 Carrier Board Configuration EEPROM

The Carrier Board **should** implement a serial EEPROM that describes the expected PCI Express link configuration. In addition this EEPROM **may** describe the expected link presence for SATA, SAS, Express Card, USB, TV-Out, VGA, LVDS, SDVO, LAN, audio, and the expected presence of miscellaneous I/O signals.

The Carrier Board Configuration EEPROM allows the ETXexpress module BIOS to set up any software configurable module features in a way that is appropriate for the Carrier board. If there is an incompatibility between the expected Carrier Board configuration and the module capabilities, an error message **may** be generated. The error messaging is module vendor specific and is not defined by this standard.

5.3.1 *EEPROM Device Information*

If the Carrier Board serial EEPROM is implemented, a two-wire serial interface device operating at a supply voltage of 3.3V **shall** be used. The two-wire interface **shall** be I^2C compatible. The device **shall** have a capacity of at least 2048 bits, and **shall** have three address inputs. A suitable device is the Ael AT24C02-2.7 or equivalent.

The Carrier Board EEPROM device, if implemented, **shall** interface to the module over the general purpose I^2C interface (ETXexpress pin names I2C_DAT and I2C_CK). The device address lines, A2, A1 and A0 **shall** be pulled to a logic high, placing the device at address 7.

Serial devices with capacity greater than 2048 bits **may** be used. If this is done, the ETXexpress Carrier Board Configuration EEPROM data structure (summarized in Table 5-14 below) **shall** occupy the top 2048 bits of the EEPROM device.

5.3.2 *EEPROM PCI Express Lane Descriptor Data Structure*

Lane numbers 0 through 31 refer to the 32 possible ETXexpress lanes. Each ETXexpress connector PCI Express lane is allocated four bytes to describe how the lanes are grouped on the module to form PCI Express links.

Of the four bytes, or 32 bits, per lane, the two most significant bytes (bit 31 down through bit 16) are reserved for link attribute information. The two least significant bytes (bit 15 through bit 0) describe the width and starting lane number of the link. This data structure allows all conceivable lane configurations to be described.

Table 5-6: Lane Descriptor Data

Link Attribute MSB	Bit 31	0: Gen 1 PCI Express link; 1: Gen 2 PCI Express link
	Bit 30	Reserved
	Bit 29	Reserved
	Bit 28	Reserved
	Bit 27	Reserved
	Bit 26	Reserved
	Bit 25	Reserved
	Bit 24	Reserved
Link Attribute LSB	Bit 23	Reserved
	Bit 22	Reserved
	Bit 21	Reserved
	Bit 20	Reserved
	Bit 19	Reserved
	Bit 18	Reserved
	Bit 17	Reserved
	Bit 16	Reserved
Link Width	Bit 15	Descriptor bits 15..8 describe the width of the PCI Express link. Possible values are 00, 01, 02, 04, 08, 10 and 20 (hex), for link widths of 0,1,2,4,8, 16 or 32 (decimal).
	Bit 14	
	Bit 13	
	Bit 12	
	Bit 11	
	Bit 10	
	Bit 9	
	Bit 8	
Link Starting Lane Number	Bit 7	Descriptor bits 7..0 describe the starting lane number of the link. If a lane is not used, then a value of 0000 0000 hex is entered for that lane number.
	Bit 6	
	Bit 5	
	Bit 4	
	Bit 3	
	Bit 2	
	Bit 1	
	Bit 0	

Table 5-7: EEPROM Data Example

Here is an EEPROM data example for four PCI Express x1 lanes and one x16 PEG interface.

Address Offset		**PCI Express Lane No.**		**ETXexpress Label**	**EEPROM Data**	
Hex	Dec	Hex	Dec		Hex	
7C	124	1F	31	PCIE 31	0000 1010	16th of 16 lanes, starting at lane 16
78	120	1E	30	PCIE 30	0000 1010	15th of 16 lanes, starting at lane 16
74	116	1D	29	PCIE 29	0000 1010	14th of 16 lanes, starting at lane 16
70	112	1C	28	PCIE 28	0000 1010	13th of 16 lanes, starting at lane 16
6C	108	1B	27	PCIE 27	0000 1010	12th of 16 lanes, starting at lane 16
68	104	1A	26	PCIE 26	0000 1010	11th of 16 lanes, starting at lane 16
64	100	19	25	PCIE 25	0000 1010	10th of 16 lanes, starting at lane 16
60	96	18	24	PCIE 24	0000 1010	9th of 16 lanes, starting at lane 16
5C	92	17	23	PCIE 23	0000 1010	8th of 16 lanes, starting at lane 16
58	88	16	22	PCIE 22	0000 1010	7th of 16 lanes, starting at lane 16
54	84	15	21	PCIE 21	0000 1010	6th of 16 lanes, starting at lane 16
50	80	14	20	PCIE 20	0000 1010	5th of 16 lanes, starting at lane 16
4C	76	13	19	PCIE 19	0000 1010	4th of 16 lanes, starting at lane 16
48	72	12	18	PCIE 18	0000 1010	3rd of 16 lanes, starting at lane 16
44	68	11	17	PCIE 17	0000 1010	2nd of 16 lanes, starting at lane 16
40	64	10	16	PCIE 16	0000 1010	1st of 16 lanes, starting at lane 16
3C	60	F	15	PCIE 15	0000 0000	Lane not used
38	56	E	14	PCIE 14	0000 0000	Lane not used
34	52	D	13	PCIE 13	0000 0000	Lane not used
30	48	C	12	PCIE 12	0000 0000	Lane not used
2C	44	B	11	PCIE 11	0000 0000	Lane not used
28	40	A	10	PCIE 10	0000 0000	Lane not used
24	36	9	9	PCIE 9	0000 0000	Lane not used
20	32	8	8	PCIE 8	0000 0000	Lane not used
1C	28	7	7	PCIE 7	0000 0000	Lane not used
18	24	6	6	PCIE 6	0000 0000	Lane not used
14	20	5	5	PCIE 5	0000 0000	Lane not used
10	16	4	4	PCIE 4	0000 0000	Lane not used
C	12	3	3	PCIE 3	0000 0103	1 lane, starting at lane 3
8	8	2	2	PCIE 2	0000 0102	1 lane, starting at lane 2
4	4	1	1	PCIE 1	0000 0101	1 lane, starting at lane 1
0	0	0	0	PCIE 0	0000 0100	1 lane, starting at lane 0

5.3.3 *SATA / SAS Device Descriptor Byte*

The configuration EEPROM **shall** use a byte to indicate how many SATA and SAS devices the Carrier Board uses, per the following table.

Table 5-8: SATA / SAS Device Descriptor Byte

Bit	Description	Value
7	SATA / SAS Channel 3	1: SAS device 0: SATA device
6		1: Connector implemented on Carrier Board 0: Not implemented
5	SATA / SAS Channel 2	1: SAS device 0: SATA device
4		1: Connector implemented on Carrier Board 0: Not implemented
3	SATA / SAS Channel 1	1: SAS device 0: SATA device
2		1: Connector implemented on Carrier Board 0: Not implemented
1	SATA / SAS Channel 0	1: SAS device 0: SATA device
0		1: Connector implemented on Carrier Board 0: Not implemented

5.3.4 *Express Card Descriptor Byte*

The configuration EEPROM **shall** use two bytes to indicate if the Carrier Board supports up to 2 Express Card slots. The following table shows the Express Card Descriptor Byte definition.

Table 5-9: Express Card Descriptor Byte

Bit	Description	Value
7	Express Card Support	1: Express Card slot implemented 0: Express Card slot not implemented
6-4	Express Card USB Port Mapping	000b – 111b indicating the USB port number mapped to this Express Card site
3	Reserved	0
2-0	Express Card PCI Express Lane Mapping	000b – 101b indicating the PCI Express Lane that is mapped to this Express Card site

5.3.5 *USB Descriptor Byte*

The configuration EEPROM **shall** use one byte to indicate how many USB ports the Carrier Board uses. Note that per the module fill order, described in Section 3.3 of this document, the USB ports **shall** be populated in a low to high manner.

Table 5-10: USB Descriptor Byte

Bit	Description	Value
7-4	Reserved	0
3-0	USB Port Count	0 - 8 indicating the number of USB ports implemented

5.3.6 *Display Descriptor Byte*

The configuration EEPROM **shall** use one byte to indicate the display options used by the Carrier Board. The following table shows the Display Descriptor Byte definition.

Table 5-11: Display Descriptor Byte

Bit	Description	Value
7	TV-Out Component Video	1: Component Video implemented 0: Component Video not implemented
6	TV-Out S-Video	1: S-Video implemented 0: S-Video not implemented
5	TV-Out Composite Video	1: Composite Video implemented 0: Composite Video not implemented
4	VGA	1: VGA implemented 0: VGA not implemented
3	LVDS Channel B	1: LVDS channel implemented 0: LVDS channel not implemented
2	LVDS Channel A	1: LVDS channel implemented 0: LVDS channel not implemented
1	SDVO Channel C	1: SDVO channel implemented 0: SDVO channel not implemented
0	SDVO Channel B	1: SDVO channel implemented 0: SDVO channel not implemented

Note: further details about the type of video signals (i.e. PAL/NTSC/ SECAM, 480p/ 720p/1080i/1080p, etc.) are beyond the scope and purpose of the configuration EEPROM.

5.3.7 *LAN Descriptor Byte*

The configuration EEPROM **shall** use one byte to indicate the LAN options used by the Carrier Board. The following table shows the LAN Descriptor Byte definition.

Table 5-12: LAN Descriptor Byte

Bit	Description	Value
7-4	Reserved	0
3	10 GBE	Reserved for future usage *1: 10 Gigabit Ethernet port implemented* *0: 10 Gigabit Ethernet port not implemented*
2	GBE 2	1: Ethernet port implemented 0: Ethernet port not implemented
1	GBE 1	1: Ethernet port implemented 0: Ethernet port not implemented
0	GBE 0	1: Ethernet port implemented 0: Ethernet port not implemented

5.3.8 *Miscellaneous I/O Descriptor Byte*

The configuration EEPROM **shall** use one byte to indicate usage by the Carrier Board of the following miscellaneous I/O signals.

- AC ’97 Digital Interface
- Watchdog Timer
- External BIOS ROM
- Thermal Protection
- Battery Low
- Suspend
- Wake

The following table shows the Miscellaneous I/O Descriptor Byte definition.

Table 5-13: Miscellaneous I/O Descriptor Byte

Bit	Description	Value
7	AC ’97 (AC_**** pins)	1: Implemented 0: Not implemented
6	Watchdog Timer (WDT)	1: Implemented 0: Not implemented
5	External BIOS ROM (BIOS_DISABLE#)	1: Implemented 0: Not implemented
4	Thermal Protection (THRM#, THERMTRIP#)	1: Implemented 0: Not implemented
3	Battery Low (BATLOW#)	1: Implemented 0: Not implemented
2	Suspend (SUS_**** pins)	1: Implemented 0: Not implemented
1	Wake 1 (WAKE1#)	1: Implemented 0: Not implemented
0	Wake 0 (WAKE0#)	1: Implemented 0: Not implemented

5.3.9 *EEPROM Memory Map*

Table 5-14: ETXexpress Carrier Board Configuration EEPROM Memory Map

EEPROM Address (Hex)	Content
FF - FE	Unsigned 16 bit checksum over the unsigned bytes at addresses 00 through FD
FD - F0	Reserved: fill with '00'
EF - E0	ASCII ID string: "COMExpressConfig"
DF	Reserved: fill with '00'
DE	SAS Device Descriptor Byte
DD	Express Card 1 Descriptor Byte
DC	Express Card 0 Descriptor Byte
DB	USB Descriptor Byte
DA	Display Descriptor Byte
D9	LAN Descriptor Byte
D8	Miscellaneous I/O Descriptor Byte
D7 - 80	Reserved: fill with '00'
7C	PCIE Lane 31 Descriptor: 4 bytes
78	PCIE Lane 30 Descriptor: 4 bytes
74	PCIE Lane 29 Descriptor: 4 bytes
70	PCIE Lane 28 Descriptor: 4 bytes
6C	PCIE Lane 27 Descriptor: 4 bytes
68	PCIE Lane 26 Descriptor: 4 bytes
64	PCIE Lane 25 Descriptor: 4 bytes
60	PCIE Lane 24 Descriptor: 4 bytes
5C	PCIE Lane 23 Descriptor: 4 bytes
58	PCIE Lane 22 Descriptor: 4 bytes
54	PCIE Lane 21 Descriptor: 4 bytes
50	PCIE Lane 20 Descriptor: 4 bytes
4C	PCIE Lane 19 Descriptor: 4 bytes
48	PCIE Lane 18 Descriptor: 4 bytes
44	PCIE Lane 17 Descriptor: 4 bytes
40	PCIE Lane 16 Descriptor: 4 bytes
3C	PCIE Lane 15 Descriptor: 4 bytes
38	PCIE Lane 14 Descriptor: 4 bytes
34	PCIE Lane 13 Descriptor: 4 bytes
30	PCIE Lane 12 Descriptor: 4 bytes
2C	PCIE Lane 11 Descriptor: 4 bytes
28	PCIE Lane 10 Descriptor: 4 bytes
24	PCIE Lane 9 Descriptor: 4 bytes
20	PCIE Lane 8 Descriptor: 4 bytes
1C	PCIE Lane 7 Descriptor: 4 bytes
18	PCIE Lane 6 Descriptor: 4 bytes
14	PCIE Lane 5 Descriptor: 4 bytes
10	PCIE Lane 4 Descriptor: 4 bytes
C	PCIE Lane 3 Descriptor: 4 bytes
8	PCIE Lane 2 Descriptor: 4 bytes
4	PCIE Lane 1 Descriptor: 4 bytes
0	PCIE Lane 0 Descriptor: 4 bytes

The EEPROM data is filled in "Little-Endian" fashion (least significant, or righost, byte in a multi-byte value goes to lower address).

5.4 Loss Budgets for High Speed Differential Interfaces

ETXexpress Module and Carrier Board insertion loss budgets for the PCI Express, SATA, USB and GBE interfaces are presented in the following sections.

The ETXexpress Module and Carrier Board insertion loss budgets were formulated to be compatible with the relevant source specifications. The source specifications vary in their treaent of insertion loss parameters. For example, the PCI Express Card Electromechanical Specification factors cross talk losses into the insertion loss budgets, but the SATA, USB and GBE source specifications do not.

For frequency dependent material losses, a rule-of-thumb insertion loss value of 0.28 dB per inch per GHz is used in all cases, representative of commonly used FR4 PCB laminates. This value is consistent with the PCI Express Card Electromechanical Specification usage (which calls out a 1.4 dB material loss for 4 inches of trace at 1.25 GHz). It is also consistent with other PICMG® specifications that use values slightly above and below this value.

Module and Carrier Board vendors **may** elect to use PCB laminates with better characteristics than common FR4. If this is done, then the trace lengths referenced in the following sections **may** be extended as long as the net insertion loss budgets are met.

Loss budgets for future generations of PCI Express (Gen 2), Ethernet (10 Gbps) and SATA (Gen 3) will be addressed in future revisions to this document.

There is no explicit ETXexpress jitter budget for the high speed differential interfaces. Designers are referred to the relevant source specifications (PCIE, SATA, USB and GBE) for system jitter budgets.

5.4.1 *PCI Express Insertion Loss Budget with Slot Card*

Figure 5-1: PCI Express Insertion Loss Budget with Slot Card

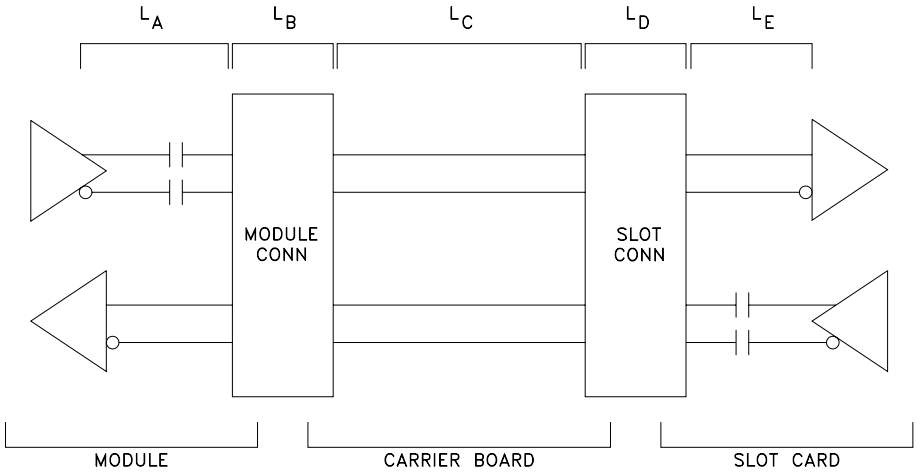


Table 5-15: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board Slot Card

Segment	Loss (dB)	Notes
L_A	3.46	Allowance for 5.15 inches of module trace @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps	1.19	From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B	0.25	ETXexpress connector at 1.25 GHz measured value.
L_C	4.40	Allowance for 9 inches of Carrier Board trace @ 0.28 dB / GHz / inch and a 1.25 dB crosstalk allowance.
L_D	1.25	PCI Express Card Electromechanical Spec Rev 1.1 “guard band” allowance for slot connector – includes 1.0 dB connector loss.
L_E	2.65	From PCI Express Card Electromechanical Spec., Rev. 1.1 (without coupling caps; L_{AR}). Implied crosstalk allowance is 1.25 dB.
Total	13.20	

The module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the module transmit path. The module transmit path insertion loss budget **shall** be 4.65 dB (3.46 dB + 1.19 dB). The module receive path insertion loss budget **shall** be 3.46 dB. ETXexpress connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are the same in this case. The Carrier Board insertion loss budget **shall** be 4.40 dB. ETXexpress connector and slot card connector losses are accounted for separately.

The slot card transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the slot card’s transmit path. The slot card’s transmit path insertion loss budget is 3.84 dB (2.65 dB + 1.19 dB) per the PCI Express Card Electromechanical Specification Revision 1.1. The slot card’s receive path insertion loss budget is 2.65 dB per the same specification. Slot card connector loss is accounted for separately.

5.4.2 *PCI Express Insertion Loss Budget with Carrier Board PCIE Device*

The insertion losses previously allowed for the slot card and slot card connector are re-allocated for use on the Carrier Board, allowing longer Carrier Board trace lengths and more Carrier Board design flexibility. The module and ETXexpress connector loss budgets remain the same.

Figure 5-2: PCI Express Insertion Loss Budget with Carrier Board PCIE Device

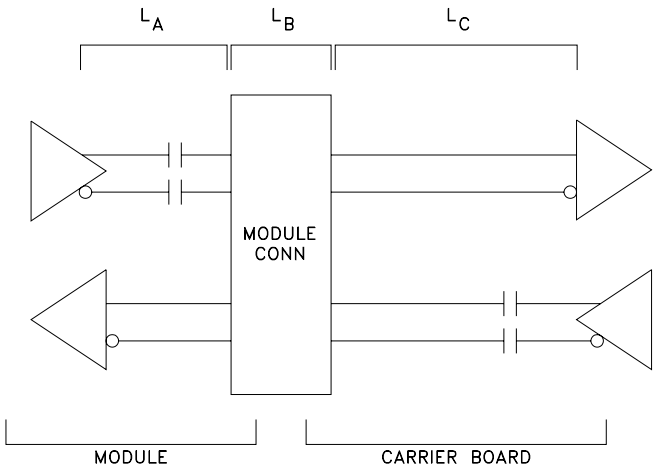


Table 5-16: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board PCIE Device

Segment	Loss (dB)	Notes
L_A	3.46	Allowance for 5.15 inches of module trace @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps	1.19	From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters ($L_{ST} – L_{SR}$). Includes crosstalk allowance of 0.79 dB.
L_B	0.25	ETXexpress connector at 1.25 GHz measured value.
L_C	8.30	Allowance for 15.85 inches of Carrier Board trace @ 0.28 dB / GHz / inch and a 2.75 dB crosstalk allowance.
Total	13.20	

The module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the module transmit path. The module transmit path insertion loss budget **shall** be 4.65 dB (3.46 dB + 1.19 dB). The module receive path insertion loss budget **shall** be 3.46 dB. ETXexpress connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Carrier Board transmit path. The Carrier Board transmit path insertion loss budget **shall** be 9.49 dB (8.30 dB + 1.19 dB). The Carrier Board receive path insertion loss **shall** be 8.30 dB. ETXexpress connector loss is accounted for separately.
.

5.4.3 *SATA Insertion Loss Budget*

The Serial ATA source specification provides insertion loss figures only for the SATA cable. There are several cable types defined with insertion losses ranging from 6 dB up to 16 dB. Cross talk losses are separate from material losses in the SATA specification.

The ETXexpress SATA Insertion loss budgets presented below represent the material losses and do not include cross talk losses. The ETXexpress SATA Insertion loss budgets are a guideline: module and Carrier Board vendors **should not** exceed the values shown in the tables below.

Figure 5-3: SATA Insertion Loss Budget

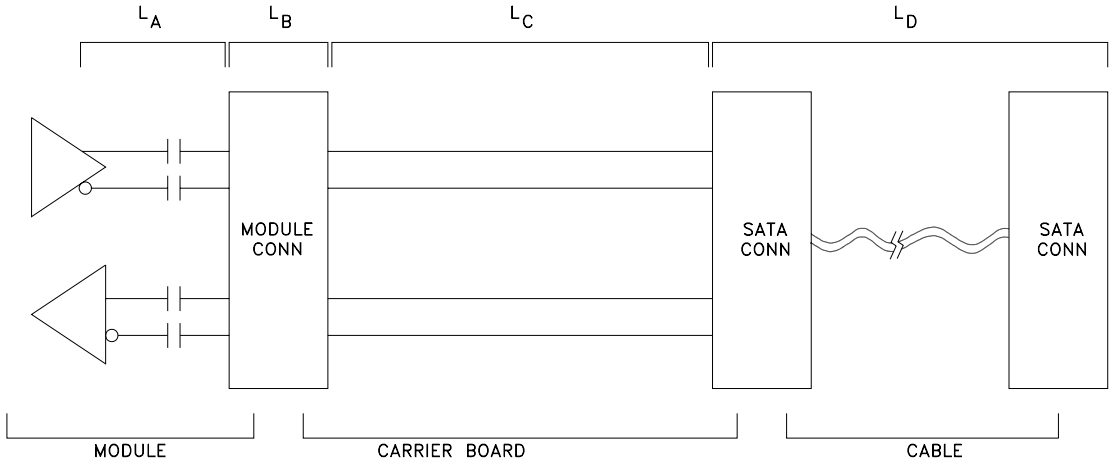


Table 5-17: SATA Gen 1 Insertion Loss Budget, 1.5 GHz

Segment	Loss (dB)	Notes
L_A	1.26	Up to 3.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.25	ETXexpress connector at 1.5 GHz measured value
L_C	3.07	Up to 7.2 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

Table 5-18: SATA Gen 2 Insertion Loss Budget, 3.0 GHz

Segment	Loss (dB)	Notes
L_A	1.68	Up to 2.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.38	ETXexpress connector at 3.0 GHz measured value
L_C	2.52	Up to 3.0 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

5.4.4 *USB Insertion Loss Budget*

Figure 5-4: USB Insertion Loss Budget

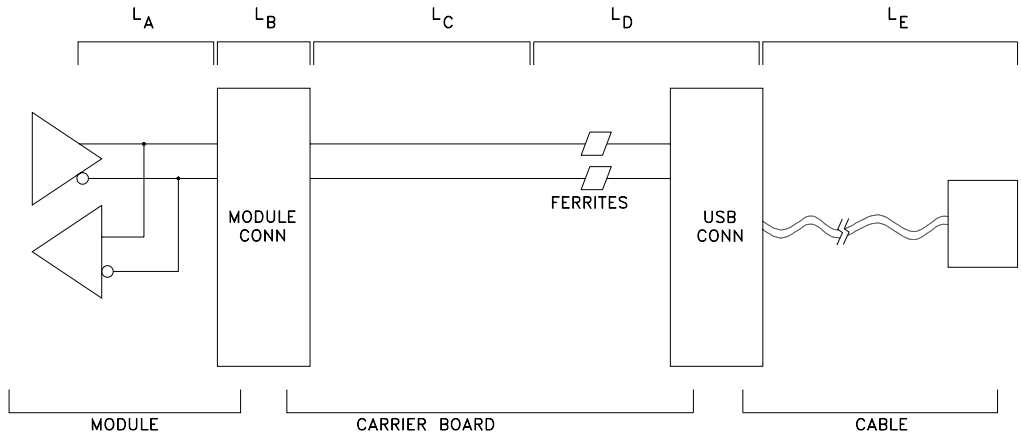


Table 5-19: USB Insertion Loss Budget, 400 MHz

Segment	Loss (dB)	Notes
L_A	0.67	Up to 6 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.05	ETXexpress connector at 400 MHz measured value
L_C	1.68	Up to 14 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	1.00	USB connector and ferrite loss
L_E	5.80	USB cable and far end connector loss, per source specification
Total	9.20	

ETXexpress USB implementations **should** conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

"Device Down" implementations, in which the USB target device is implemented on the Carrier Board, **may** add the ferrite and USB connector insertion loss values to the Carrier Board budget. The Carrier Board insertion loss budget then becomes $L_C + L_D$, or 2.68 dB.

5.4.5 *10/100/1000 Ethernet Insertion Loss Budget*

Figure 5-5: 10/100/1000 Ethernet Insertion Loss Budget

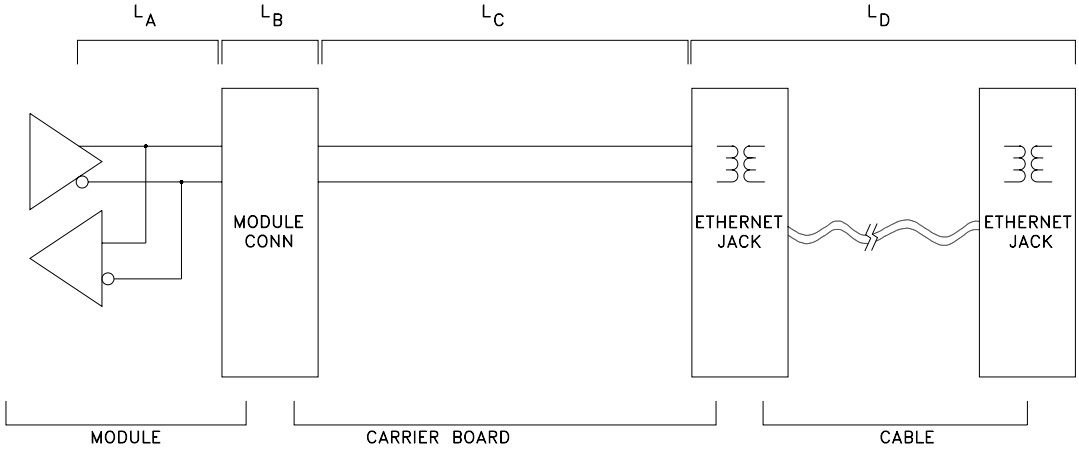


Table 5-20: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz

Segment	Loss (dB)	Notes
L_A	0.08	Up to 3 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.02	ETXexpress connector at 100 MHz measured value
L_C	0.15	Up to 5 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	24.00	Cable and cable connectors, integrated magnetics, per source spec.
Total	24.25	

ETXexpress Ethernet implementations **should** conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gb Ethernet specification.

"Device Down" implementations, in which the Ethernet target device is implemented on the Carrier Board (for instance, an Ethernet switch), **may** add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the Carrier Board budget. This insertion loss value is typically 1 dB. The Carrier Board insertion loss budget then becomes L_C + 1 dB, or 1.15 dB.

5.5 PCI Bus Implementation

5.5.1 *Carrier Board PCI Resource Allocation*

On ETXexpress modules with Type 2 and 3 pin-outs four off-module PCI devices **shall** be supported. The off-module devices are referred to as Slot 0,1,2,3 devices. They **may** be PCI slots (connectors) on the Carrier Board, or they **may** be actual PCI devices on the Carrier Board itself. The PCI implementation **shall** support four REQ / GNT pairs for off-module use.

The following table summarizes how resources are allocated on a Carrier Board implementation.

Table 5-21: Carrier Board PCI Resource Allocation

Slot / Device Signal	Slot / Device 0	Slot / Device 1	Slot / Device 2	Slot / Device 3
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
PCI Clock	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTD# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#
REQ0# (if used)	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#
REQ1# (if used)	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#
REQ2# (if used)	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#
REQ3# (if used)	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#
GNT0# (if used)	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#
GNT1# (if used)	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#
GNT2# (if used)	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#
GNT3# (if used)	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#

5.5.2 *PCI Clocks*

ETXexpress specifies only a single copy of the PCI clock for off-module use. If only one Carrier Board PCI device is implemented, then that single clock **may** be routed to the device. If more than one Carrier Board PCI device is implemented, then the Carrier Board **should** replicate the PCI clock using a zero delay buffer.

The PCI Local Bus Specification requires that PCI clocks be synchronous within a 2 ns window at the destination devices; that the maximum propagation delay for the clock be 10 ns, and that PCI slot based add-on cards implement a PCI clock trace length of 2.5 inches.

ETXexpress Carrier Board implementations **should** allow 1.6 ns +/- 0.1 ns for the PCI clock propagation delay from the ETXexpress module connector pin to the destination device pin. Propagation delay varies with construction details such as trace geometry, PCB stack up, and PCB material dielectric constant. Propagation delay values of 140 ps / inch to 180 ps / inch are common for outer layer traces. A propagation delay value of 180 ps / inch is common for inner layer traces. Using 180 ps /inch as the propagation delay value for an inner layer Carrier Board PCI clock, then the ETXexpress Carrier Board delay of 1.6 ns works out to 8.88 inches of trace.

If the destination device is on an add on card, then the propagation delay associated with the 2.5 inches of add on card trace are deducted from the 1.6 ns. Using 160 ps / inch as a typical value for an outer layer slot card clock trace, the 2.5 inches of slot card clock trace length work out to a propagation delay of 0.4 ns. The Carrier Board PCI clock delay in this example would be 1.6 ns – 0.4 ns or 1.2 ns.

The following definitions and equations apply:

$_D$ Propagation delay: module PCI clock source to on-module PCI device

$_C$ Propagation delay: module PCI clock source to module connector PCI clock pin

T_{CD} Propagation delay: module connector to Carrier Board device
Fixed by ETXexpress Specification at 1.6 ns

T_{CS} Propagation delay: module connector to slot connector pin

L_{SD} Length: slot card connector pin to slot card device
Fixed by PCI Local Bus Specification at 2.5 inches

P_{SD} Inverse propagation speed: slot card connector pin to slot card device
(units of time / length)
Determined by slot card PCB design; typical value 160 ps / inch

$_D = _C + T_{CD}$

$_D = _C + T_{CS} + L_{SD} * P_{SD}$

$T_{CS} = T_{CD} – L_{SD}*P_{SD}$

The parameters $_D$ and $_C$ apply to module designs. Module designers **should** minimize $_C$, and then arrange that $_D$ satisfies the relation $_D = _C + T_{CD}$.

Figure 5-6: PCI Clocks — Carrier Board PCI Device

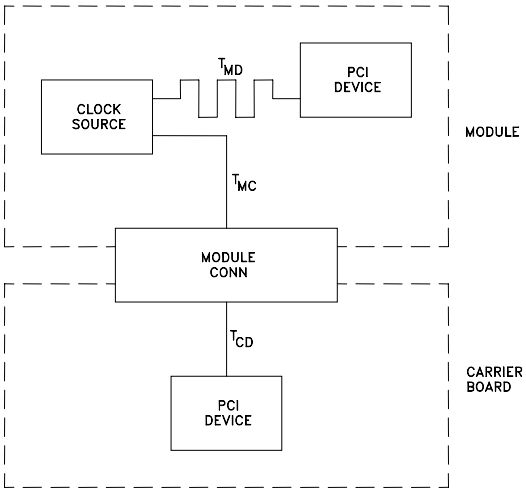
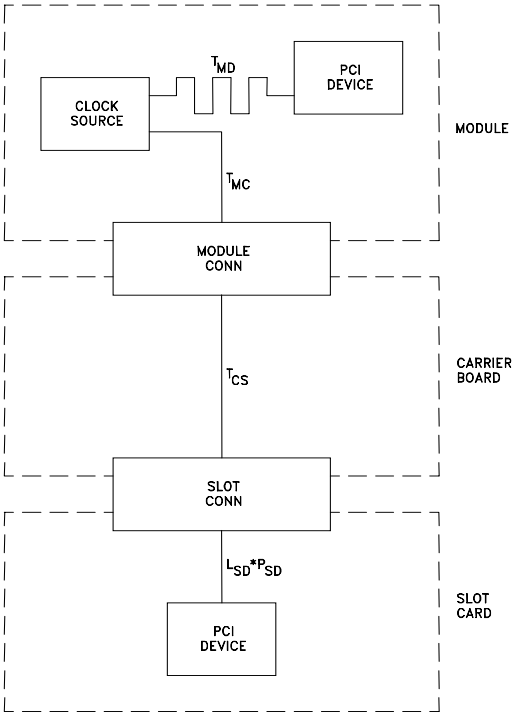


Figure 5-7: PCI Clocks — Slot Card PCI Device



5.6 Carrier Board LPC Devices

Carrier Board LPC devices **should** be clocked with the LPC clock provided by the module interface. LPC clock length guidelines are the same as those for the PCI clock.

Carrier Board LPC devices **should** be reset with signal CB_RESET#.

5.7 10 Gigabit Ethernet Option

Modules that use Pin-out Type 3 or 5 **may** implement a 10 Gigabit / sec Ethernet option by remapping the pins used for the GBE1 and GBE2 ports. The 10 Gigabit pin usage is to be defined in a future specification update.

Table 5-22: 10 Gigabit Ethernet Pin Mapping

Row C Pin	GBE1 Pin Use	10 Gigabit Pin Use
C1	GND (FIXED)	GND
C2	GBE1_ACT#	To be defined in a future ETXexpress Revision
C3	GBE1_MDI3-	
C4	GBE1_MDI3+	
C5	GBE1_LINK100#	
C6	GBE1_MDI2-	
C7	GBE1_MDI2+	
C8	GBE1_LINK1000#	
C9	GBE1_MDI1-	
C10	GBE1_MDI1+	
C11	GND (FIXED)	GND
DL0-	GBE1_MDI0-	
DL0+	GBE1_MDI0+	
GND	GBE1_LINK#	
NC	RSVD	

Row D Pin	GBE2 Pin Use	10 Gigabit Pin Use
D1	GND (FIXED)	GND
D2	GBE2_ACT#	To be defined in a future ETXexpress Revision
D3	GBE2_MDI3-	
D4	GBE2_MDI3+	
D5	GBE2_LINK100#	
D6	GBE2_MDI2-	
D7	GBE2_MDI2+	
D8	GBE2_LINK1000#	
D9	GBE2_MDI1-	
D10	GBE2_MDI1+	
D11	GND (FIXED)	GND
D12	GBE2_MDI0-	
D13	GBE2_MDI0+	
D14	GBE2_LINK#	
D15	GBE2_CTREF	

5.8 Watchdog Timer

ETXexpress modules **may** implement a watchdog timer output to the Carrier Board. If the watchdog timer (WDT) is implemented, it **should** have the characteristics described below.

5.8.1 *Output Options and Characteristics*

The watchdog **should** implement the following output options:

- Reset: the module **shall** reset. Module pins PCI_RST# , IDE_RST# and CB_RESET# **shall** be pulsed low. The module WDT pin goes high until the unit resets.
- NMI (non-maskable interrupt) is generated. The module WDT pin goes high and stays high until cleared by software.
- Output to module WDT pin only. The WDT pin stays high until cleared by software.
- Disabled: the module WDT pin is driven low.

The above output options **may** be realized by software configurable hardware or by module build options. The watchdog output **shall** come up as a logic low and **shall** be disabled upon power-on-reset (VCC_12V power cycle) or external system reset (when SYS_RST# pin is toggled low by external hardware). The watchdog **may** be enabled by BIOS or system software. If the watchdog is enabled and times out, the module WDT pin **shall** be driven to a logic high level and **shall** remain high for at least one microsecond.

5.8.2 *Watchdog Enable and Strobe*

Typically, the watchdog parameters (output options, enabling, enable delay, timeout delay) are managed by the module BIOS, often via a BIOS setup screen. The regular watchdog strobes to prevent a watchdog timeout are typically handled by the module's application software. There **may** be BIOS abstractions to isolate the application software from the watchdog hardware.

The software programmable Watchdog Enable Delay is the time between when the watchdog is enabled by firmware and when the first watchdog strobe is needed to prevent a watchdog time out. The enable delay allows time for the operating system to boot and the application to load and initialize.

After the initial Enable Delay, the enabled watchdog must be periodically strobed by software to prevent a watchdog timeout. The Strobe Interval **shall** be software programmable.

Recommended ranges in enable delay and max strobe periods are given in the following table.

Table 5-23: Watchdog Enable and Strobe Parameter Range

	Min Value	**Max Value**
Enable Delay	1 second	10 minutes
Strobe Interval	0.1 second	10 minutes

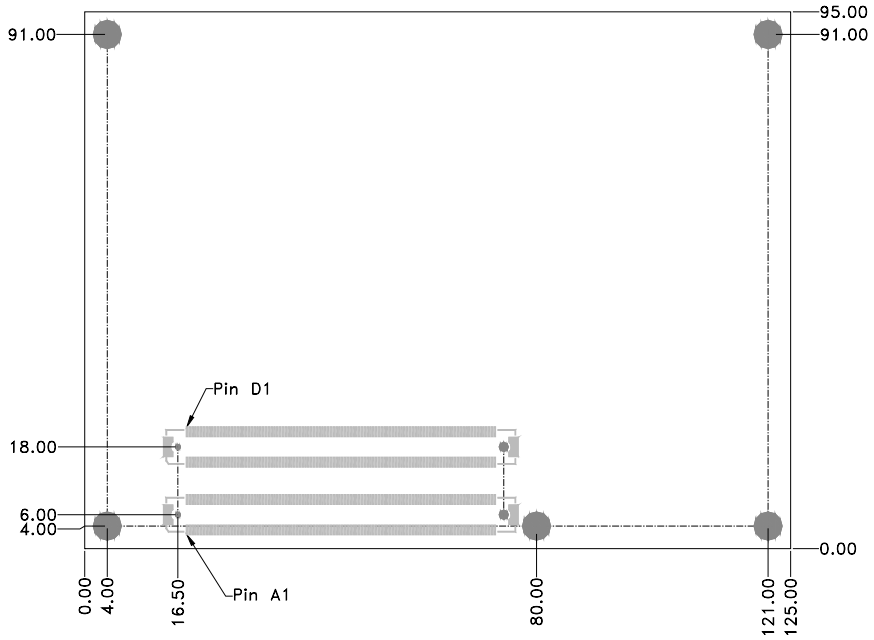
6 Mechanical Specifications

6.1 Module Size — Basic Module

The PCB size for the Basic Module **shall** be 125mm x 95mm. The PCB thickness **may** be 2mm to allow high layer count stack-ups and facilitate a standard ‘z’ dimension between the Carrier Board and the top of the heat-spreader. (See Section 6.8, “Heat-Spreader”).

The holes shown in this drawing are intended for mounting the module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers **shall** be used to attach the heat-spreader to the module.

Figure 6-1: Basic Module Form Factor



All dimensions are shown in millimeters.

Tolerances **shall** be ± 0.25mm [±0.010"], unless noted otherwise. The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00] and [16.50, 18.00]) **shall** be ± 0.10mm [±0.004"].

The 440 pin connector pair **shall** be mounted on the backside of the PCB and is seen “through” the board in this view.

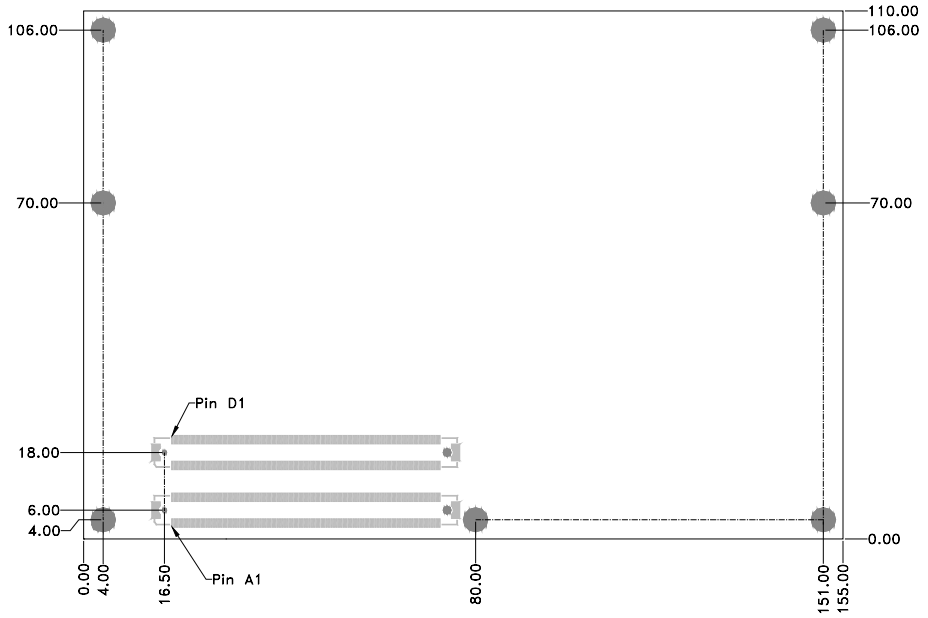
The 5 mounting holes shown **shall** use 6mm diameter pads and **shall** have 2.7mm plated holes, for use with 2.5mm hardware. The pads **shall** be tied to the PCB ground plane.

6.2 Module Size — Extended Module

The PCB size for the Extended Module **shall** be 155mm x 110mm. The PCB thickness **may** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader. (See Section 6.8, "Heat-Spreader").

The holes shown in this drawing are intended for mounting the module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers **shall** be used to attach the heat-spreader to the module.

Figure 6-2: Extended Module Form Factor



All dimensions are shown in millimeters.

Tolerances **shall** be ± 0.25mm [±0.010"], unless noted otherwise. The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00] and [16.50, 18.00]) **shall** be ± 0.10mm [±0.004"].

The 440 pin connector pair **shall** be mounted on the backside of the PCB and is seen "through" the board in this view.

The seven mounting holes shown **shall** use 6 mm diameter pads and have 2.7 mm plated holes, for use with 2.5 mm hardware. The pads **shall** be tied to the PCB ground plane.

6.3 Module Connector

The module connector for Pin-out Types 2 through 5 **shall** be a 440-pin receptacle that is composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle. The pair of connectors **may** be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Module Pin-out Type 1 **shall** use a single 220-pin, 0.5 mm pitch receptacle. The connectors **shall** be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds.

Sources for the individual 220-pin receptacle are

AMP / Tyco	3-1318490-6	0.5 mm pitch Free Height 220 pin 4H Receptacle, or equivalent
AMP / Tyco	8-1318490-6	0.5 mm pitch Free Height 220 pin 4H Recepacle, or equivalent (same as previous part, but with anti-wicking solution applied)

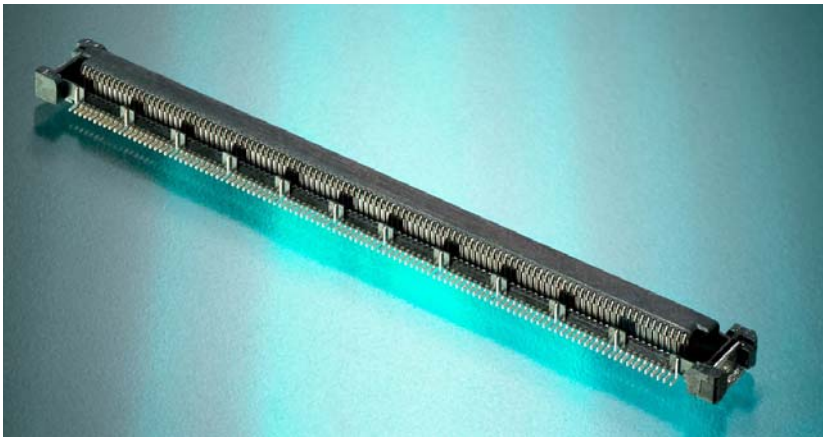
A source for the combined 440-pin receptacle (composed of 2 pieces of the 220 pin receptacle held by a carrier) is:

AMP / Tyco 3-1827231-6 0.5mm pitch Free Height 440 pin 4H Receptacle or equivalent.

Note: the part number above shown with a leading ‘8’ has an anti-wicking solution applied that **may** help in processing with an aggressive flux. The other versions of the parts **may** also be made available with this solution by the vendor.

The module connector is a receptacle by virtue of the vendor’s technical definition of a receptacle, and to some users it looks like a plug.

Figure 6-3: Module Receptacle



6.4 Carrier Board Connector

The Carrier Board connector for module Pin-out Types 2 through 5 **shall** be a 440-pin plug that is composed of 2 pieces of a 220-pin, 0.5 mm pitch plug. The pair of connectors **may** be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Carrier Boards intended only for use with Pin-out Type 1 modules **may** use a single 220-pin, 0.5 mm pitch plug. The connectors **shall** be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds. The Carrier Board plugs are available in a variety of heights. The Carrier Board **shall** use either the 5mm or 8mm heights.

A source for the individual 5 mm stack height 220 pin plug is:

AMP / Tyco 3-1827253-6 0.5 mm pitch Free Height 220 pin 5H Plug or equivalent

A source for the combined 5mm stack height 440-pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) is:

AMP / Tyco 3-1827233-6 0.5 mm pitch Free Height 440 pin 5H Plug or equivalent.

A source for the individual 8 mm stack height 220 pin plug is:

AMP / Tyco 3-1318491-6 0.5 mm pitch Free Height 220 pin 8H Plug or equivalent

AMP / Tyco 8-1318491-6 0.5 mm pitch Free Height 220 pin 8H Plug or equivalent
(same as previous part, but with anti-wicking solution applied)

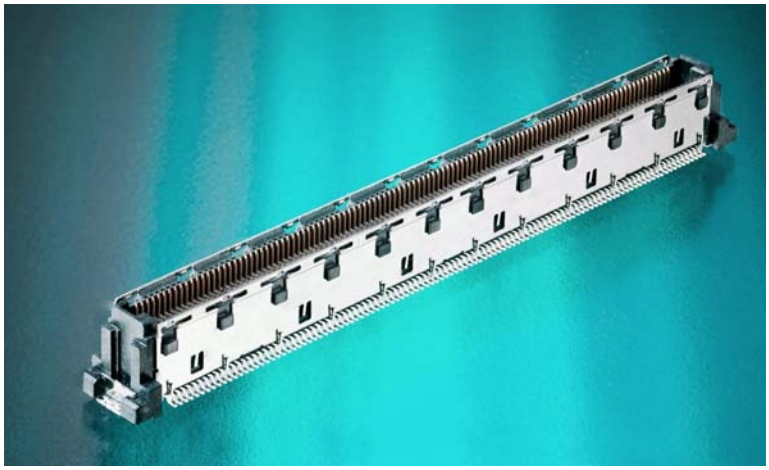
A source for the combined 8 mm stack height 440 pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) is:

AMP / Tyco 3-5353652-6 0.5 mm Free Height 440 pin 8H Plug or equivalent.

Note: the part number above shown with a leading ‘8’ has an anti-wicking solution applied that **may** help in processing with an aggressive flux. The other versions of the parts **may** also be made available with this solution by the vendor.

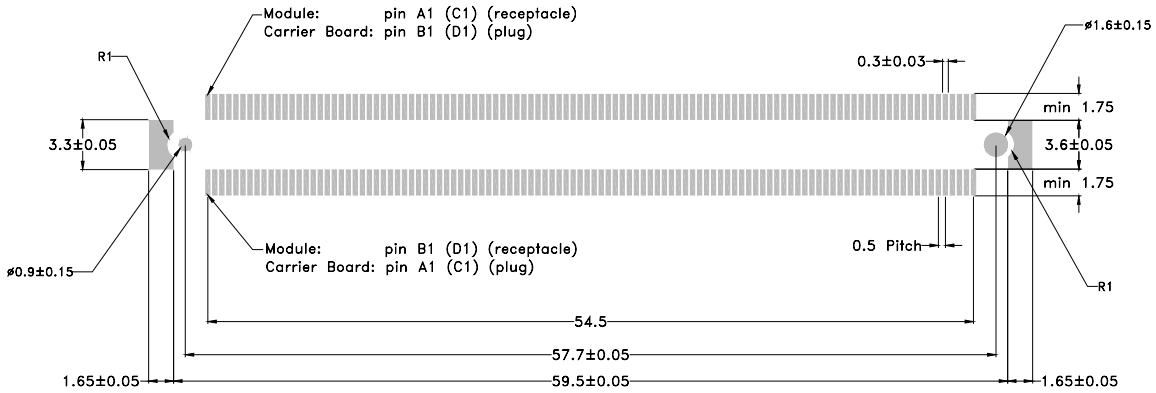
The Carrier Board connector is a plug by virtue of the vendor’s technical definition of a plug, and to some users it looks like a receptacle.

Figure 6-4: Carrier Board Plug (8-mm Version)



6.5 Connector PCB Pattern

Figure 6-5: Connector PCB Pattern

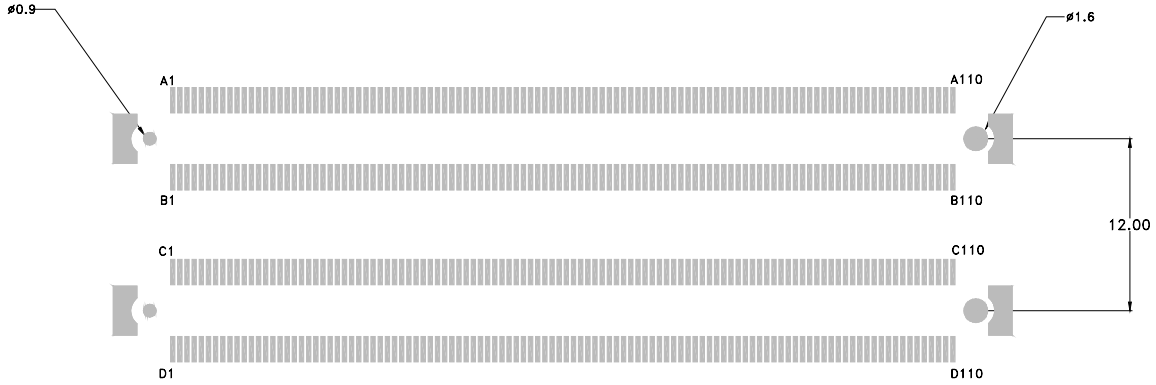


All dimensions in mm.

6.6 Module Connector Pin Numbering

Pin numbering for 440-pin module receptacle. This is a top view of the receptacle, looking into the receptacle, as mounted on the backside of the module.

Figure 6-6: Module Connector Pin Numbering

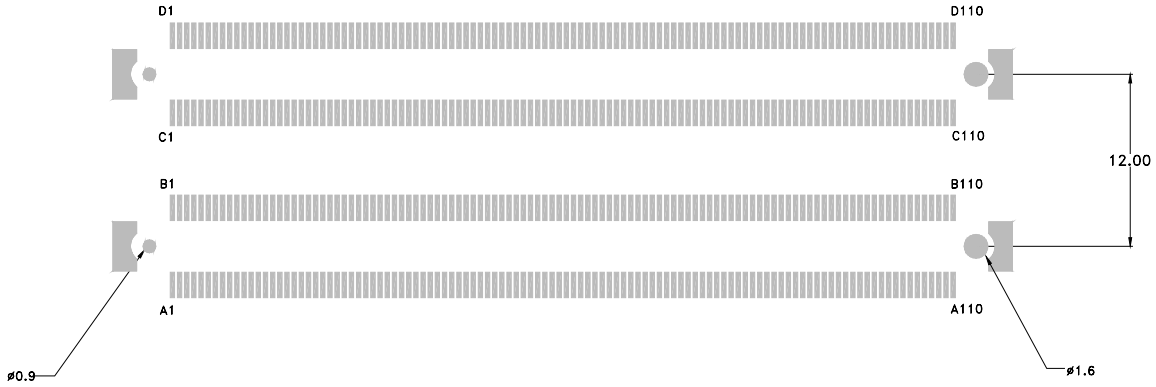


All dimensions in mm.

6.7 Carrier Board Connector Pin Numbering

Pin numbering for 440-pin carrier-board plug. This is a top view, looking into the plug as mounted on the Carrier Board.

Figure 6-7: Carrier Board Connector Pin Numbering



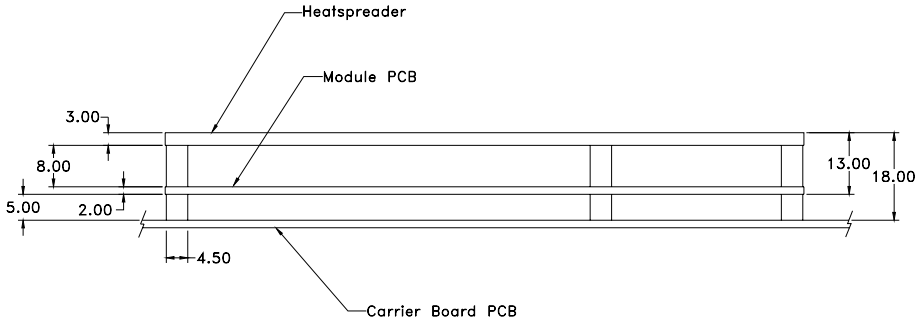
All dimensions in mm.

6.8 Heat-Spreader

Modules **should** be equipped with a heat-spreader. This heat-spreader by it self does not constitute the complete thermal solution for a module but provides a common interface between modules and implementation-specific thermal solutions.

The overall module height from the bottom surface of the module board to the heat-spreader top surface **shall** be 13 mm for both the Basic and Extended Modules. The module PCB and heat-spreader plate thickness are vendor implementation specific, however, a 2-mm PCB with a 3-mm heat-spreader **may** be used which allows use of readily available standoffs.

Figure 6-8: Overall Height for Heat-Spreader in Basic and Extended Modules



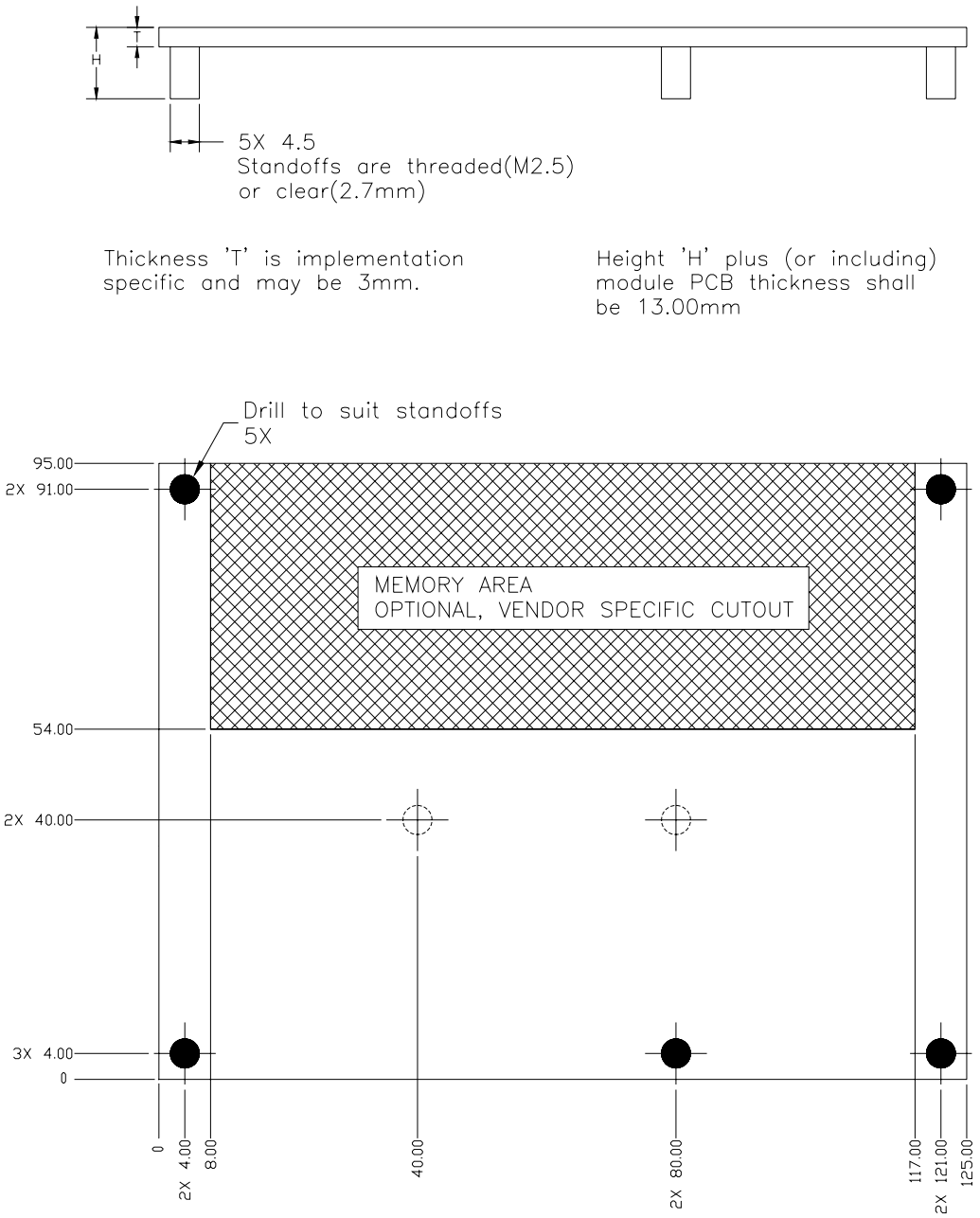
All dimensions in mm.

Tolerances (unless otherwise specified):
Z (height) dimensions **should** be ± 0.8mm [±0.031”] from top of Carrier Board to top of heat-spreader.
Heat-spreader surface **should** be flat within 0.2mm [.008"] after assembly.
Interface surface finish **should** have a maximum roughness average (R_a) of 1.6µm [63µin].

The critical dimension in Figure 6-8 is the module PCB bottom side to heat-spreader top side. This dimension **shall** be 13.00mm ± 0.65mm [±0.026”].

Figure 6-8 shows a cross section of a module and heat-spreader assembled to a Carrier Board using the 5mm stack height option. If 8mm Carrier Board connectors are used, the overall assembly height increases from 18.00mm to 21.00mm.

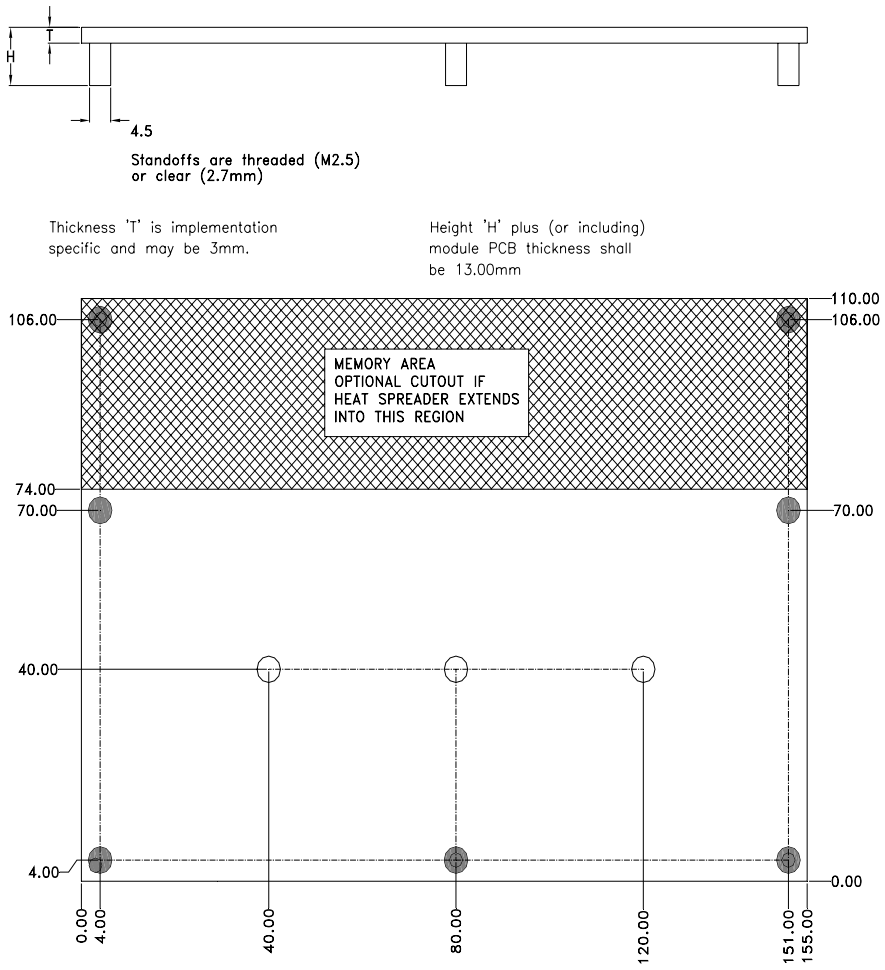
Figure 6-9: Basic Module Heat-Spreader



All dimensions are in mm. X-Y tolerances **shall** be ± 0.3mm [±0.012"].

The interior holes at coordinates (40, 40) and (80, 40) are tapped through holes with a M2.5 thread. The interior holes do not receive standoffs. These holes **may** be sealed on the module side by an adhesive backed foil, or they **may** be blind tapped holes with a minimum thread depth of 2.5 mm. They are intended to allow additional attachment points to the heat-spreader from outside the module.

Figure 6-10: Heat-Spreader Specification for Extended Module



All dimensions are in mm. X-Y tolerances **shall** be ± 0.3mm [±0.012"].

The Extended Module heat-spreader **shall** have minimum X-Y dimensions of 155 mm x 74 mm, as per the clear area in the figure above. The hatched area indicates the PCB area that **may** be used for memory modules. The Extended Module heat-spreader **may** extend into the memory area. This extension is vendor specific. The maximum X-Y extent of the Extended Module heat-spreader **shall** be 155mm x 110mm.

The interior holes at coordinates (40, 40), (80, 40) and (120,40) are tapped through holes with a M2.5 thread. The interior holes do not receive standoffs. These holes **may** be sealed on the module side by an adhesive backed foil, or they **may** be blind tapped holes with a minimum thread depth of 2.5 mm. They are intended to allow additional attachment points to the heat-spreader from outside the module.

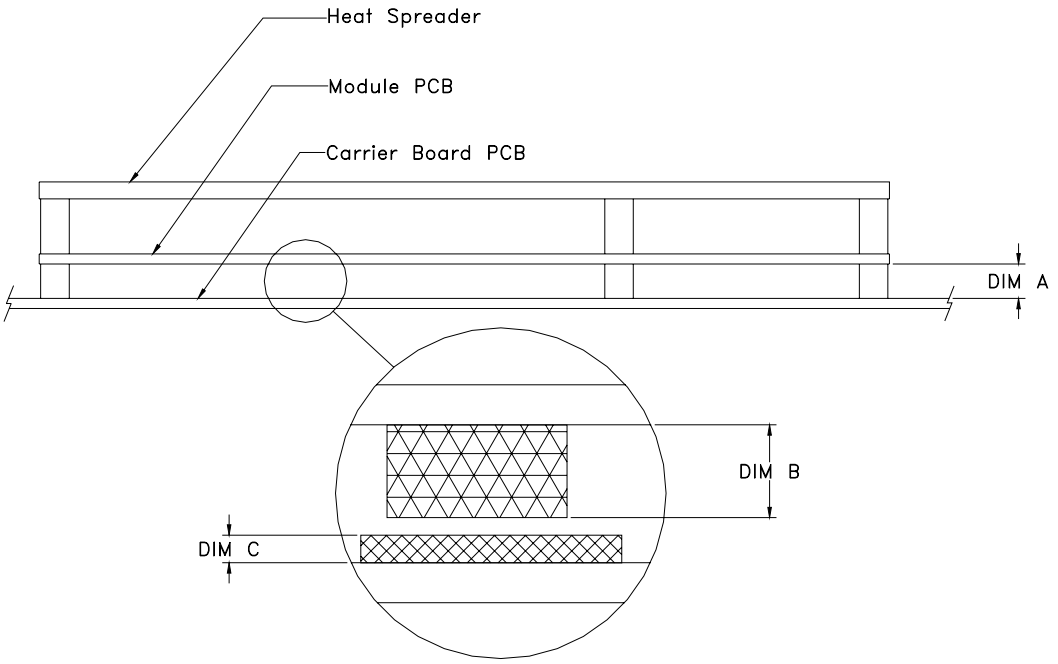
6.9 Component Height — Module Back and Carrier Board Top

Parts mounted on the backside of the module (in the space between the bottom surface of the module PCB and the Carrier Board) **shall** have a maximum height of 3.8 mm (dimension 'B' in Figure 6-11).

With the 5 mm stack option, the clearance between the Carrier Board and the bottom surface of the module's PCB is 5 mm (dimension 'A' in Figure 6-11). Using the 5 mm stack option, components placed on the Carrier Board topside under the module envelope **shall** be limited to a maximum height of 1 mm (dimension 'C' in Figure 6-11), with the exception of the mating connectors. Using Carrier Board topside components up to 1mm allows a gap of 0.2 mm between Carrier Board module bottom side components. This **may not** be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height **should** be restricted to a value less than 1mm that yields a clearance that is sufficient for the application.

If the Carrier Board uses the 8 mm stack option (dimension 'A' in Figure 6-11), then the Carrier Board topside components within the module envelope **shall** be limited to a height of 4 mm (dimension 'C' in Figure 6-11), with the exception of the mating connectors. Using Carrier Board topside components up to 4mm allows a gap of 0.2 mm between Carrier Board topside components and module bottom side components. This **may not** be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height **should** be restricted to a value less than 4 mm that yields a clearance that is sufficient for the application.

Figure 6-11: Component Clearances Underneath Module



7 Electrical Specifications

7.1 Input Power — General Considerations

The Basic and Extended Module modules **shall** use a single main power rail with a nominal value of +12V.

Two additional rails are specified: a +5V standby power rail and a +3V battery input to power the module Real-time Clock (RTC) circuit in the absence of other power sources. The +5V standby rail **may** be left unconnected on the Carrier Board if the standby functions are not required by the application. Likewise, the +3V battery input **may** be left open if the application does not require the RTC to keep time in the absence of the main and standby sources. There **may** be module specific concerns regarding storage of system setup parameters that **may** be affected by the absence of the +5V standby and / or the +3V battery.

The rationale for this power-delivery scheme is:

- Module pins are scarce. It is more pin-efficient to bring power in on a higher voltage rail.
- Single supply operation is attractive to many users.
- Lithium ion battery packs for mobile systems are most prevalent with a +14.4V output. This is well suited for the +12V main power rail.
- Contemporary chipsets have no power requirements for +5V other than to provide a reference voltage for +5V tolerant inputs. No ETXexpress module pins are allocated to accept +5V except for the +5V standby pins. In the case of an ATX supply, the switched (non standby) +5V line would not be used for the ETXexpress module, but it might be used elsewhere on the Carrier Board.

7.2 Input Power — Basic and Extended Modules

The module connector pins limit the amount of power that can be brought into the ETXexpress modules. The limits are different for module Pin-out Types 1 and for Pin-out Types 2 through 5 as Pin-out Type 1 has fewer pins available.

Table 7-1: Input Power — Pin-out Type 1 (Single Connector, 220 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	10.5	12	11.4 - 12.6	11.4	+/- 100	120	85%	101
VCC_5V_SBY	2	5	4.75 – 5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0 - 3.3		+/- 20			

Table 7-2: Input Power — Pin-out Type 2,3,4,5 Modules (Dual Connector, 440 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	16.5	12	11.4 - 12.6	11.4	+/- 100	188	85%	160
VCC_5V_SBY	2	5	4.75 – 5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0 - 3.3		+/- 20			

7.3 Input Power — Sequencing

ETXexpress input power sequencing requirements are as follows:

VCC_RTC	**shall** come up at the same time or before VCC_5V_SBY comes up.
VCC_5V_SBY	**shall** come up at the same time or before VCC_12V comes up.
PWROK	**shall** be active at the same time or after VCC_12V comes up.
PWROK	**shall** be inactive at the same time or before VCC_12V goes down.
VCC_12V	**shall** go down at the same time or before VCC_5V_SBY goes down.
VCC_5V_SBY	**shall** go down at the same time or before VCC_RTC goes down.

Figure 7-1: Power Sequencing

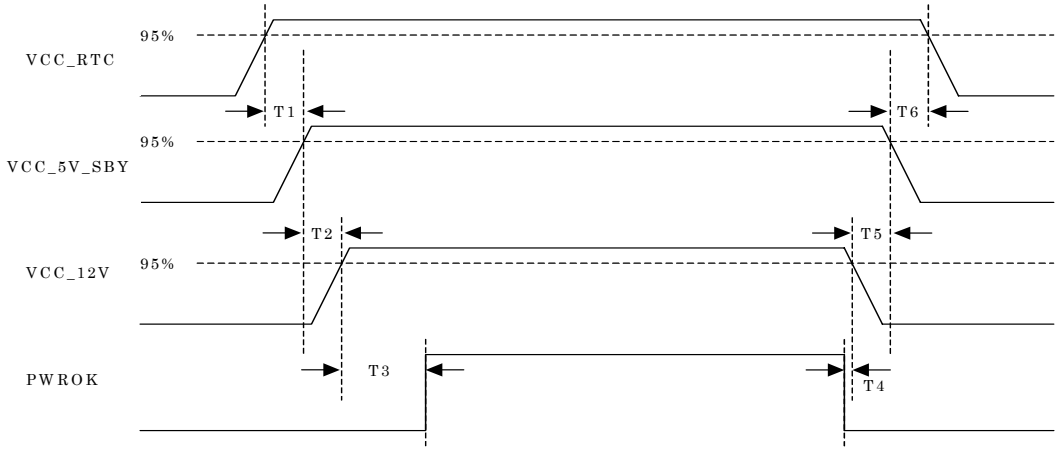


Table 7-3: Power Sequencing

T1	VCC_RTC rise to VCC_5V_SBY rise	≥ 0 ms
T2	VCC_5V_SBY rise to VCC_12V rise	≥ 0 ms
T3	VCC_12V rise to PWROK rise	≥ 0 ms
T4	PWROK fall to VCC_12V fall	≥ 0 ms
T5	VCC_12V fall to VCC_5V_SBY fall	≥ 0 ms
T6	VCC_5V_SBY fall to VCC_RTC fall	≥ 0 ms

7.4 Signal Integrity Requirements

The signal groups listed in the following table have signal-integrity concerns that **should** be accounted for in module and carrier-board designs. A general description is shown in the table for reference only. The designer **should** consult the relevant interface specification documents for complete information.

Table 7-4: Signal Integrity Requirements

Signal Group	General Description	Source Spec Reference
Analog VGA	75-ohm single ended ground-referenced lines. Generous isolation recommended.	
Component and Composite video	75-ohm single ended ground-referenced lines. Generous isolation recommended.	
Gigabit Ethernet	Differential pairs	IEEE 802.3 Specification
LVDS	100-ohm edge coupled differential pairs	National Semiconductor LVDS web site
PCI Bus	Circa 60 ohm single-ended	PCI SIG - PCI Local Bus Spec. Rev. 2.3
PCI and LPC clocks	50-ohm single ended ground-referenced	
PCI Express	Differential pairs	PCI SIG - PCI Express Specification
PCI Express clocks	100 ohm edge couple differential pair, ground-referenced	
Serial ATA	Differential pairs	SATA Specification
USB	Differential pairs	USB 2.0 Specification

8 Environmental Specifications

8.1 Thermal Specification

8.1.1 Objectives

Thermal specification requirements set forth here serve two objectives:

1. To provide a method through which any ETXexpress module's thermal performance can be specified and verified against a common reference.
2. To provide a method of thermal specification that is independent of the particular components used on the module.

These objectives are limited to the modules' heat-spreader interface, and primary heat sources are limited to the module itself and ambient air.

8.1.2 Definitions

Tcase. This is the temperature of the outside surface of the module heat-spreader plate.

Tcase_max. This is defined as the maximum temperature allowed for the heat-spreader of the module. This maximum temperature is directly tied to maximum allowed junction temperatures of the chips that are in contact with the heat-spreader.

Tcase_min. This is defined as the minimum temperature allowed for the heat-spreader of the module. This temperature is directly tied to minimum allowed junction temperatures of the chips that are in contact with the heat-spreader.

M. This is defined as the point on the heat-spreader where the maximum case temperature must be measured. The module manufacturer **should** indicate the location of this point on the module's heat-spreader and/or in its product documentation.

Tambient_max. This is defined as the maximum temperature of the air directly surrounding the module, allowed for the operation of the module.

Tambient_min. This is defined as the minimum temperature of the air directly surrounding the module, allowed for the operation of the module.

TDPmax. This is defined as the maximum power dissipation of the module for design of a thermal solution to guarantee that the module operates within the manufacturer's specifications. TDP stands for thermal design power.

Tcpu_junction. The junction temperature of the processor. Tcpu_junction can be measured in many processors by accessing an on-die thermal diode. Refer to the manufacturer datasheet for information on how to access the thermal diode. In some instances, software provided by the processor manufacturer or a third party **may** be used in conjunction with hardware on the module / carrier assembly to monitor the temperature of the processor. Verification of an internal thermal diode accuracy **should** be done and certified by the OEM. With verified accuracy of the diode, validation with software can then be done by end users.

Tcpu_junction_max. The maximum junction temperature for the processor as specified in the silicon manufacturer's datasheet. The module thermal solution (i.e. heat-spreader and heatsink) **shall** keep the processor junction temperature at or below the Tcpu_junction_max. Note that some manufacturers do not specify maximum junction temperatures but specify maximum case temperatures instead.

Tcpu_case. The CPU package case temperature, as specified in the silicon vendor's data sheet. Note that Tcpu_case and T_case refer to different locations in the ETXexpress module system.

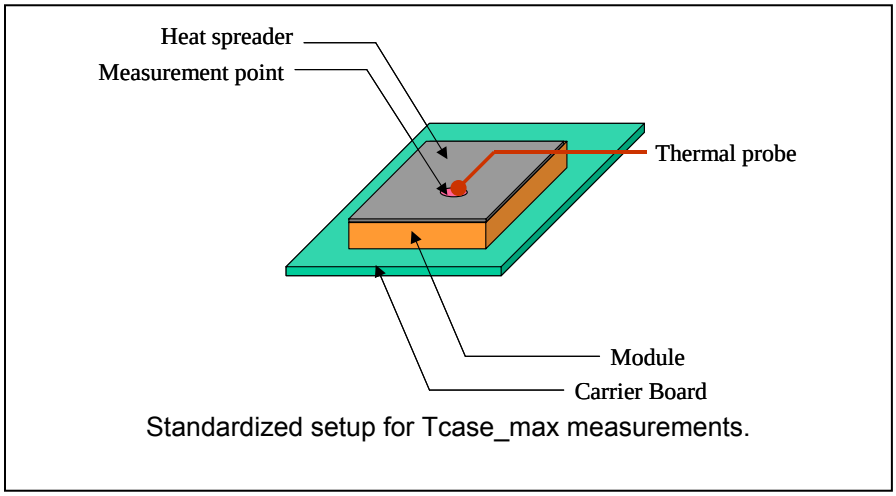
Tcpu_case_max. The maximum CPU package case temperature for the processor as specified in the silicon manufacturer's datasheet. The module's thermal solution (i.e. heat-spreader and heatsink) **shall** keep the processor case temperature at or below the Tcpu_case_max. Note that some manufacturers do not specify maximum case temperatures but specify maximum junction temperatures instead.

The ultimate goal of the system thermal solution is to ensure that Tcpu_junction or Tcpu_case, whichever applies to the CPU at hand, remain below the maximum levels specified by the CPU vendor. Similar concerns apply to other high dissipation components in the module system.

8.1.3 Tcase_max Measurement Setup

Measurements for Tcase_max **should** be performed according to a standardized method and under TDPmax conditions. The following figure depicts the standardized measurement setup for Tcase_max measurements.

Figure 8-1: Tcase_Max Measurement Point



Standardized setup for Tcase_max measurements.

This schematic illustration shows the module heat-spreader, the module, and the Carrier Board. Not shown is the user-specific cooling solution that **shall** attach to the heat-spreader. Modules are not normally operated without a cooling solution attached.

The measurement point (M) **should** be specified, either through a permanent marker on the module's heat-spreader, or through a mechanical drawing in the product's support documentation.

8.1.4 Module Thermal Specification Requirements

A module manufacturer **should** specify Tcase_max, Tcase_min, Tambient_max, Tambient_min, TDPmax and M (the Tcase_max measurement point).

A module manufacturer **may** specify Tcpu_junction_max and maximum junction temperatures of other critical chips on the module. In this case, the module vendor **should** provide software to read the junction temperature of the CPU and **may** do the same for the other critical chips. In that case, the module vendor **shall** ensure that the software is properly calibrated and that the junction temperature readings are accurate.

The efficiency of the module thermal characteristics has an impact on the module's MTBF (Mean Time Between Failure). Higher junction temperatures result in a shorter silicon life. Module vendors **should** provide MTBF information.

8.2 Humidity

The module humidity tolerance **shall** be 0 to 95% humidity, non-condensing.

8.3 Shock and Vibration

The shock and vibration characteristics of a system built with a ETXexpress module will vary depending on system-implementation details. These details include size, rigidity, and mounting configuration of the Carrier Board and the thermal solution. There is no explicit shock and vibration specification that ETXexpress modules are required to meet.

If all available ETXexpress module and heat-spreader attachment points are used, then a ETXexpress based system **should** be capable of excellent shock and vibration performance.

9 Appendix A — Pin-out Summary Tables for Types 1-5

Table 9-1: Pin-out Type 1 — 220 Pins

GB Ethernet		**AC97**		**SATA / SAS**		**IDE**		**PCI Express**		**PCI**		**USB**	
1 Port		**1 Port**		**4 Channels**				**6 Lanes**				**8 Ports**	
GBE0_MDI[0:3]-+	8	AC_RST#	1	SATA[0:3]_TX+-	8			PCIE_TX[0:5]+-	12			USB[0:7]+-	16
GBE0_ACT#	1	AC_SYNC	1	SATA[0:3]_RX+-	8			PCIE_RX[0:5]+-	12				
GBE0_LINK#	1	AC_BIT_CLK	1	ATA_ACT#	1							USB_0_1_OC#	1
GBE0_LINK100#	1	AC_SDOUT	1					PCIE_CLK_REF+-	2			USB_2_3_OC#	1
GBE0_LINK1000#	1	AC_SDIN[0:2]	3									USB_4_5_OC#	1
GBE0_CTREF	1											USB_6_7_OC#	1
	13		7		17		0		26		0		20
LVDS Flat Panel		**Express Card Support**		**VGA / TV Out**		**LPC**		**Miscellaneous**		**Power and System Management**		**Power**	
2 Ports		**2 Ports**		**1 Port / 1 Port**									
LVDS_A[0:3]+-	8	EXCD_CPPE[0:1]#	2	VGA_RED	1	LPC_AD[3:0]	4	I2C_CK	1	PWRBTN#	1	Fixed GND	24
LVDS_A_CK+-	2	EXCD_RST[0:1]#	2	VGA_BLU	1	LPC_FRAME#	1	I2C_DAT	1	SUS_S3#	1	Additional GND	3
LVDS_B[0:3]+-	8			VGA_GRN	1	LPC_DRQ[0:1]#	2	SPKR	1	SUS_S4#	1		
LVDS_B_CK+-	2			VGA_HSYNC	1	LPC_SERIRQ	1	BIOS_DISABLE#	1	SUS_S5 #	1	VCC_12V	21
LVDS_VDD_EN	1			VGA_VSYNC	1	LPC_CLK	1	WDT	1	BATLOW#	1		
LVDS_BKLT_EN	1			VGA_I2C_CLK	1							VCC5_SBY	4
LVDS_BKLT_CTRL	1			VGA_I2C_DAT	1					THRM#	1		
LVDS_I2C_CK	1									THRMTRP#	1	VCC_RTC	1
LVDS_I2C_DAT	1									SMB_CK	1		
				TV_DAC_A	1			GPO[0:3]	4	SMB_DAT	1		
				TV_DAC_B	1			GPI[0:3]	4	SMB_ALERT#	1		
				TV_DAC_C	1					PWR_OK	1		
								KBD_RST#	1	SYSRESET#	1		
								KBD_A20GATE	1	SUS_STAT#	1		
										CB_RESET#	1		
										WAKE0#	1		
								Reserved	5	WAKE1#	1		
	25		4		10		9		20		16		53

Table 9-2: Pin-out Type 2 — 440 Pins

GB Ethernet		**AC97**		**SATA / SAS**		**IDE**		**PCI Express**		**PCI**		**USB**	
1 Port		**1 Port**		**4 Channels**		**1 Port**		**22 Lanes**		**4 Bus Masters**		**8 Ports**	
GBE0_MDI[0:3]-+	8	AC_RST#	1	SATA[0:3]_TX+-	8	IDE_D[0:15]	16	PCIE_TX[0:5]+-	12	PCI_AD[0..31]	32	USB[0:7]+-	16
GBE0_ACT#	1	AC_SYNC	1	SATA[0:3]_RX+-	8	IDE_A[0:2]	3	PCIE_RX[0:5]+-	12	PCI_C/BE[0..3]#	4		
GBE0_LINK#	1	AC_BIT_CLK	1	ATA_ACT#	1	IDE_IOW#	1			PCI_SERR#	1	USB_0_1_OC#	1
GBE0_LINK100#	1	AC_SDOUT	1			IDE_IOR#	1	PEG_TX[0:15]+-	32	PCI_RESET#	1	USB_2_3_OC#	1
GBE0_LINK1000#	1	AC_SDIN[0:2]	3			IDE_REQ	1	PEG_RX[0:15]+-	32	PCI_IRQ[A:D]#	4	USB_4_5_OC#	1
GBE0_CTREF	1					IDE_ACK#	1			PCI_FRAME#	1	USB_6_7_OC#	1
						IDE_CS1#	1	PCIE_CLK_REF+-	2	PCI_STOP#	1		
						IDE_CS3#	1			PCI_DEVSEL#	1		
						IDE_IORDY	1	PEG_LANE_RV#	1	PCI_LOCK#	1		
						IDE_RESET#	1	PEG_ENABLE#	1	PCI_PERR#	1		
						IDE_IRQ	1			PCI_IRDY#	1		
						IDE_CBLID#	1	SDVO_DATA	1	PCI_TRDY#	1		
								SDVO_CK	1	PCI_PAR	1		
										PCI_CLK	1		
										PCI_REQ[0..3]#	4		
										PCI_GNT[0..3]#	4		
										PCI_CLKRUN#	1		
										PCI_PME#	1		
										PCI_M66EN	1		
	13		7		17		29		94		62		20
LVDS Flat Panel		**Express Card Support**		**VGA / TV Out**		**LPC**		**Miscellaneous**		**Power and System Management**		**Power**	
2 Ports		**2 Ports**		**1 Port / 1 Port**									
LVDS_A[0:3]+-	8	EXCD_CPPE[0:1]#	2	VGA_RED	1	LPC_AD[3:0]	4	I2C_CK	1	PWRBTN#	1	Fixed GND	48
LVDS_A_CK+-	2	EXCD_RST[0:1]#	2	VGA_BLU	1	LPC_FRAME#	1	I2C_DAT	1	SUS_S3#	1	Additional GND	16
LVDS_B[0:3]+-	8			VGA_GRN	1	LPC_DRQ[0:1]#	2	SPKR	1	SUS_S4#	1		
LVDS_B_CK+-	2			VGA_HSYNC	1	LPC_SERIRQ	1	BIOS_DISABLE#	1	SUS_S5 #	1	VCC_12V	33
LVDS_VDD_EN	1			VGA_VSYNC	1	LPC_CLK	1	WDT	1	BATLOW#	1		
LVDS_BKLT_EN	1			VGA_I2C_CLK	1							VCC5_SBY	4
LVDS_BKLT_CTRL	1			VGA_I2C_DAT	1			TYPE[0:2]	3	THRM#	1		
LVDS_I2C_CK	1									THRMTRP#	1	VCC_RTC	1
LVDS_I2C_DAT	1									SMB_CK	1		
				TV_DAC_A	1			GPO[0:3]	4	SMB_DAT	1		
				TV_DAC_B	1			GPI[0:3]	4	SMB_ALERT#	1		
				TV_DAC_C	1					PWR_OK	1		
								KBD_RST#	1	SYSRESET#	1		
								KBD_A20GATE	1	SUS_STAT#	1		
										CB_RESET#	1		
										WAKE0#	1		
								Reserved	14	WAKE1#	1		
	25		4		10		9		32		16		102

Table 9-3: Pin-out Type 3 — 440 Pins

GB Ethernet		**AC97**		**SATA / SAS**		**IDE**		**PCI Express**		**PCI**		**USB**	
3 Ports		**1 Port**		**4 Channels**				**22 Lanes**		**4 Bus Masters**		**8 Ports**	
GBE0_MDI[0:3]+-	8	AC_RST#	1	SATA[0:3]_TX+-	8			PCIE_TX[0:5]+-	12	PCI_AD[0..31]	32	USB[0:7]+-	16
GBE0_ACT#	1	AC_SYNC	1	SATA[0:3]_RX+-	8			PCIE_RX[0:5]+-	12	PCI_C/BE[0..3]#	4		
GBE0_LINK100#	1	AC_BIT_CLK	1	ATA_ACT#	1					PCI_SERR#	1	USB_0_1_OC#	1
GBE0_LINK1000#	1	AC_SDOUT	1					PEG_TX[0:15]+-	32	PCI_RESET#	1	USB_2_3_OC#	1
GBE0_LINK#	1	AC_SDIN[0:2]	3					PEG_RX[0:15]+-	32	PCI_IRQ[A:D]#	4	USB_4_5_OC#	1
GBE0_CTREF	1									PCI_FRAME#	1	USB_6_7_OC#	1
								PCIE_CLK_REF+-	2	PCI_STOP#	1		
GBE1_MDI[0-3]+-	8									PCI_DEVSEL#	1		
GBE1_ACT#	1							PEG_LANE_RV#	1	PCI_LOCK#	1		
GBE1_LINK1000#	1							PEG_ENABLE#	1	PCI_PERR#	1		
GBE1_LINK100#	1									PCI_IRDY#	1		
GBE1_LINK#	1							SDVO_DATA	1	PCI_TRDY#	1		
								SDVO_CK	1	PCI_PAR	1		
GBE2_MDI[0-3]+-	8									PCI_CLK	1		
GBE2_ACT#	1									PCI_REQ[0..3]#	4		
GBE2_LINK100#	1									PCI_GNT[0..3]#	4		
GBE2_LINK1000#	1									PCI_CLKRUN#	1		
GBE2_LINK#	1									PCI_PME#	1		
GBE2_CTREF	1									PCI_M66EN	1		
	38		7		17		0		94		62		20
LVDS Flat Panel		**Express Card Support**		**VGA / TV Out**		**LPC**		**Miscellaneous**		**Power and System Management**		**Power**	
2 Ports		**2 Ports**		**1 Port / 1 Port**									
LVDS_A[0:3]+-	8	EXCD_CPPE[0:1]#	2	VGA_RED	1	LPC_AD[3:0]	4	I2C_CK	1	PWRBTN#	1	Fixed GND	48
LVDS_A_CK+-	2	EXCD_RST[0:1]#	2	VGA_BLU	1	LPC_FRAME#	1	I2C_DAT	1	SUS_S3#	1	Additional GND	16
LVDS_B[0:3]+-	8			VGA_GRN	1	LPC_DRQ[0:1]#	2	SPKR	1	SUS_S4#	1		
LVDS_B_CK+-	2			VGA_HSYNC	1	LPC_SERIRQ	1	BIOS_DISABLE#	1	SUS_S5 #	1	VCC_12V	33
LVDS_VDD_EN	1			VGA_VSYNC	1	LPC_CLK	1	WDT	1	BATLOW#	1		
LVDS_BKLT_EN	1			VGA_I2C_CLK	1							VCC5_SBY	4
LVDS_BKLT_CTRL	1			VGA_I2C_DAT	1			TYPE[0:2]	3	THRM#	1		
LVDS_I2C_CK	1									THRMTRP#	1	VCC_RTC	1
LVDS_I2C_DAT	1									SMB_CK	1		
				TV_DAC_A	1			GPO[0:3]	4	SMB_DAT	1		
				TV_DAC_B	1			GPI[0:3]	4	SMB_ALERT#	1		
				TV_DAC_C	1					PWR_OK	1		
								KBD_RST#	1	SYSRESET#	1		
								KBD_A20GATE	1	SUS_STAT#	1		
										CB_RESET#	1		
										WAKE0#	1		
								Reserved	18	WAKE1#	1		
	25		4		10		9		36		16		102

Table 9-4: Pin-out Type 4 — 440 Pins

GB Ethernet		**AC97**		**SATA / SAS**		**IDE**		**PCI Express**		**PCI**		**USB**	
1 Port		**1 Port**		**4 Channels**		**1 Port**		**32 Lanes**				**8 Ports**	
GBE0_MDI[0:3]-+	8	AC_RST#	1	SATA[0:3]_TX+-	8	IDE_D[0:15]	16	PCIE_TX[0:31]+-	64			USB[0:7]+-	16
GBE0_ACT#	1	AC_SYNC	1	SATA[0:3]_RX+-	8	IDE_A[0:2]	3	PCIE_RX[0:31]+-	64				
GBE0_LINK#	1	AC_BIT_CLK	1	ATA_ACT#	1	IDE_IOW#	1					USB_0_1_OC#	1
GBE0_LINK100#	1	AC_SDOUT	1			IDE_IOR#	1	PCIE_CLK_REF+-	2			USB_2_3_OC#	1
GBE0_LINK1000#	1	AC_SDIN[0:2]	3			IDE_REQ	1					USB_4_5_OC#	1
GBE0_CTREF	1					IDE_ACK#	1	PEG_LANE_RV#	1			USB_6_7_OC#	1
						IDE_CS1#	1	PEG_ENABLE#	1				
						IDE_CS3#	1						
						IDE_IORDY	1	SDVO_DATA	1				
						IDE_RESET#	1	SDVO_CK	1				
						IDE_IRQ	1						
						IDE_CBLID#	1						
	13		7		17		29		134		0		20
LVDS Flat Panel		**Express Card Support**		**VGA / TV Out**		**LPC**		**Miscellaneous**		**Power and System Management**		**Power**	
2 Ports		**2 Ports**		**1 Port / 1 Port**									
LVDS_A[0:3]+-	8	EXCD_CPPE[0:1]#	2	VGA_RED	1	LPC_AD[3:0]	4	I2C_CK	1	PWRBTN#	1	Fixed GND	48
LVDS_A_CK+-	2	EXCD_RST[0:1]#	2	VGA_BLU	1	LPC_FRAME#	1	I2C_DAT	1	SUS_S3#	1	Additional GND	16
LVDS_B[0:3]+-	8			VGA_GRN	1	LPC_DRQ[0:1]#	2	SPKR	1	SUS_S4#	1		
LVDS_B_CK+-	2			VGA_HSYNC	1	LPC_SERIRQ	1	BIOS_DISABLE#	1	SUS_S5 #	1	VCC_12V	33
LVDS_VDD_EN	1			VGA_VSYNC	1	LPC_CLK	1	WDT	1	BATLOW#	1		
LVDS_BKLT_EN	1			VGA_I2C_CLK	1							VCC5_SBY	4
LVDS_BKLT_CTRL	1			VGA_I2C_DAT	1			TYPE[0:2]	3	THRM#	1		
LVDS_I2C_CK	1									THRMTRP#	1	VCC_RTC	1
LVDS_I2C_DAT	1									SMB_CK	1		
				TV_DAC_A	1			GPO[0:3]	4	SMB_DAT	1		
				TV_DAC_B	1			GPI[0:3]	4	SMB_ALERT#	1		
				TV_DAC_C	1					PWR_OK	1		
								KBD_RST#	1	SYSRESET#	1		
								KBD_A20GATE	1	SUS_STAT#	1		
										CB_RESET#	1		
										WAKE0#	1		
								Reserved	36	WAKE1#	1		
	25		4		10		9		54		16		102

Table 9-5: Pin-out Type 5 — 440 Pins

GB Ethernet		**AC97**		**SATA / SAS**		**PATA**		**PCI Express**		**PCI**		**USB**	
3 Ports		**1 Port**		**4 Channels**				**32 Lanes**				**8 Ports**	
GBE0_MDI[0:3]+-	8	AC_RST#	1	SATA[0:3]_TX+-	8			PCIE_TX[0:31]+-	64			USB[0:7]+-	16
GBE0_ACT#	1	AC_SYNC	1	SATA[0:3]_RX+-	8			PCIE_RX[0:31]+-	64				
GBE0_LINK100#	1	AC_BIT_CLK	1	ATA_ACT#	1							USB_0_1_OC#	1
GBE0_LINK1000#	1	AC_SDOUT	1					PCIE_CLK_REF+-	2			USB_2_3_OC#	1
GBE0_LINK#	1	AC_SDIN[0:2]	3									USB_4_5_OC#	1
GBE0_CTREF	1							PEG_LANE_RV#	1			USB_6_7_OC#	1
								PEG_ENABLE#	1				
GBE1_MDI[0-3]+-	8												
GBE1_ACT#	1							SDVO_DATA	1				
GBE1_LINK100#	1							SDVO_CK	1				
GBE1_LINK1000#	1												
GBE1_LINK#	1												
GBE2_MDI[0-3]+-	8												
GBE2_ACT#	1												
GBE2_LINK100#	1												
GBE2_LINK1000#	1												
GBE2_LINK#	1												
GBE2_CTREF	1												
	38		7		17		0		134		0		20

LVDS Flat Panel		**Express Card Support**		**VGA / TV Out**		**LPC**		**Miscellaneous**		**Power and System Management**		**Power**	
2 Ports		**2 Ports**		**1 Port / 1 Port**									
LVDS_A[0:3]+-	8	EXCD_CPPE[0:1]#	2	VGA_RED	1	LPC_AD[3:0]	4	I2C_CK	1	PWRBTN#	1	Fixed GND	48
LVDS_A_CK+-	2	EXCD_RST[0:1]#	2	VGA_BLU	1	LPC_FRAME#	1	I2C_DAT	1	SUS_S3#	1	Additional GND	16
LVDS_B[0:3]+-	8			VGA_GRN	1	LPC_DRQ[0:1]#	2	SPKR	1	SUS_S4#	1		
LVDS_B_CK+-	2			VGA_HSYNC	1	LPC_SERIRQ	1	BIOS_DISABLE#	1	SUS_S5 #	1	VCC_12V	33
LVDS_VDD_EN	1			VGA_VSYNC	1	LPC_CLK	1	WDT	1	BATLOW#	1		
LVDS_BKLT_EN	1			VGA_I2C_CLK	1							VCC5_SBY	4
LVDS_BKLT_CTRL	1			VGA_I2C_DAT	1			TYPE[0:2]	3	THRM#	1		
LVDS_I2C_CK	1									THRMTRP#	1	VCC_RTC	1
LVDS_I2C_DAT	1									SMB_CK	1		
				TV_DAC_A	1			GPO[0:3]	4	SMB_DAT	1		
				TV_DAC_B	1			GPI[0:3]	4	SMB_ALERT#	1		
				TV_DAC_C	1					PWR_OK	1		
								KBD_RST#	1	SYSRESET#	1		
								KBD_A20GATE	1	SUS_STAT#	1		
										CB_RESET#	1		
										WAKE0#	1		
								Reserved	40	WAKE1#	1		
	25		4		10		9		58		16		102