GRBM2K 技术说明 v120

1， 技术指标（需扩展指标可来电咨询）

（1）CPU：2K1000 (商业级、工业级、军用级)

（2）内存：2GB DDR3 存储器

（3）NOR FLASH：2MB 用于存放引导

（4）NAND_ FLASH：256MB 用于存放系统映像及数据

（5）模块接口：2 个千兆电口

1 路 SATA 接口

4 路 USB 接口

pcie 总线、支持 x4、x2、x1

局部总线 LIO,可配置为 8 路串口等

4 个串口

2 个 IIC,2 个 can 口,1 个 spi 口

8 个 GPIO,4 个 PWM

引出 DVO0,DVO1：支持底板扩展配置为 DVI/HDMI/VGA 等显示接口

（6）尺寸：84 x 55mm

（7）电源：单电源输入 +5~12V，功耗约 7W

（8）散热要求：需要使用散热片或风扇

（9）工作温度：-40℃～+70℃（工业级，器件指标-40℃～+85℃）

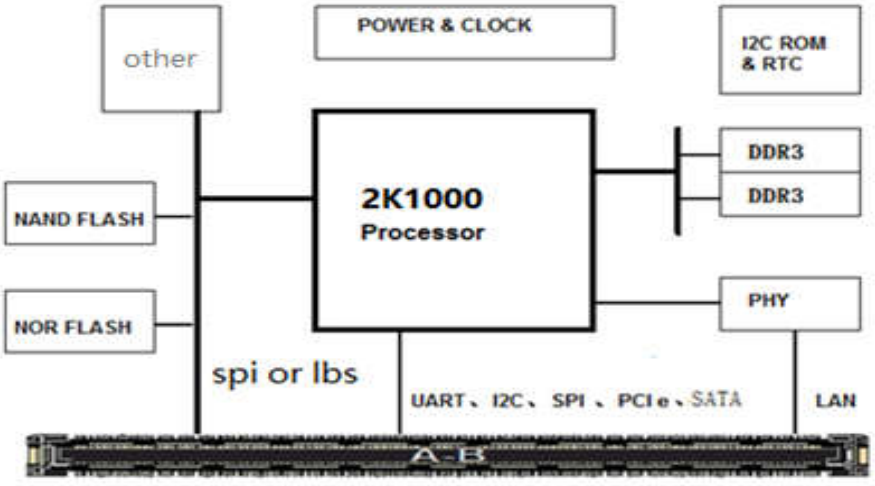
（10）系统支持 Linux 或 vxWorks 等

（11）国产化指标：模块分为”100%国产化”版本和”99%国产化”版本,接口兼容

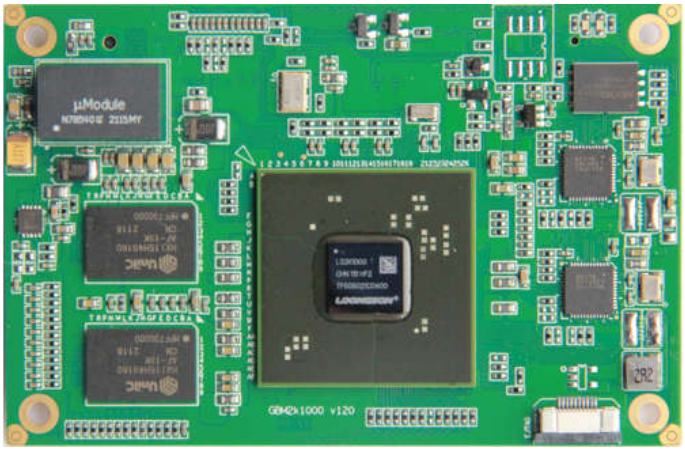
（12）接口定义见附录一

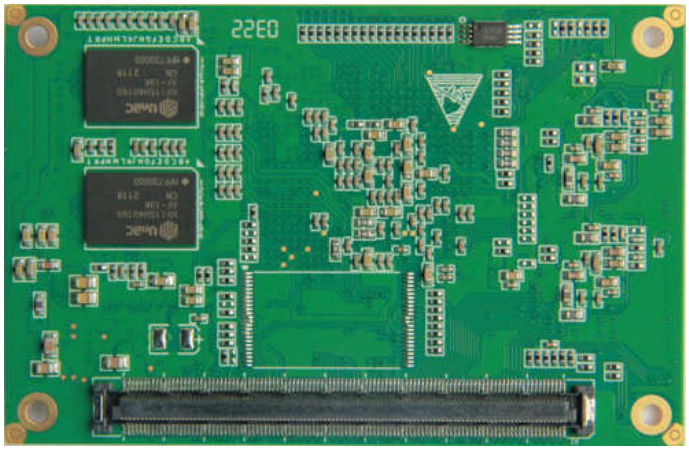
2， 产品介绍

a， 原理框图



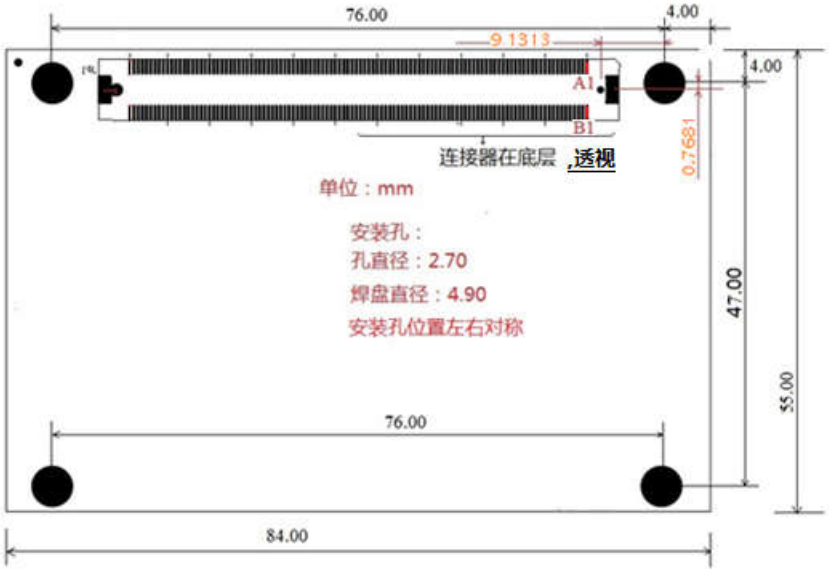
b， 模块图片





c， 结构说明

模块外形尺寸如下图（顶视图），详细的结构尺寸见用户手册。



附录：

一，接口定义(定义描述见用户手册)

J1					
序号	定义	参考电平	序号	定义	参考电平
A1	GND		B1	GND	
A2	LS2K_GPIO41	3.3V	B2	LS2K_GPIO39	3.3V
A3	LS2K_GPIO40	3.3V	B3	LS2K_GPIO38	3.3V
A4	LS2K_CAN1_TX	3.3V	B4	LS2K_GPIO37	3.3V
A5	LS2K_CAN1_RX	3.3V	B5	LS2K_GPIO36	3.3V
A6	LS2K_CAN0_TX	3.3V	B6	LS2K_SPI_SCK	3.3V
A7	LS2K_CAN0_RX	3.3V	B7	LS2K_SPI_SDO	3.3V
A8	LS2K_PWM1	3.3V	B8	LS2K_SPI_SDI	3.3V
A9	/EXT_RST_IN	3.3V	B9	LS2K_SPI_CSN2	3.3V
A10	LS2K_IIC0_SCL	3.3V	B10	LS2K_SPI_CSN3	3.3V
A11	GND		B11	GND	
A12	LS2K_IIC0_SDA	3.3V	B12	LS2K_PWM3	3.3V
A13	LS2K_IIC1_SCL/PWM2	3.3V	B13	LIO_WR/PWR0	3.3V
A14	LS2K_IIC1_SDA	3.3V	B14	LIO_RD	3.3V
A15	LS2K_GPIO0	3.3V	B15	LIO_A0	3.3V
A16	LS2K_HDA_SDI0	3.3V	B16	LIO_A1	3.3V
A17	LS2K_HDA_SDO	3.3V	B17	LIO_A2	3.3V
A18	LS2K_HDA_RST	3.3V	B18	LIO_A3	3.3V
A19	LS2K_HDA_BITCLK	3.3V	B19	LIO_A4	3.3V
A20	LS2K_HDA_SYNC	3.3V	B20	LIO_A5	3.3V
A21	GND		B21	GND	
A22	LIO_AD08/UART	3.3V	B22	LIO_A6	3.3V
A23	LIO_AD09/UART	3.3V	B23	LIO_DIR/UART	3.3V
A24	LIO_AD10/UART	3.3V	B24	LIO_ADLOCK/UART	3.3V
A25	LIO_AD11/UART	3.3V	B25	LIO_CSn	3.3V
A26	LIO_AD12/UART	3.3V	B26	LIO_AD00/UART	3.3V
A27	LIO_AD13/UART	3.3V	B27	LIO_AD01/UART	3.3V
A28	LIO_AD14/UART	3.3V	B28	LIO_AD02/UART	3.3V
A29	LIO_AD15/UART	3.3V	B29	LIO_AD03/UART	3.3V
A30	LIO_DEN/UART	3.3V	B30	LIO_AD04/UART	3.3V
A31	GND		B31	GND	
A32	UART5_RXD	3.3V	B32	LIO_AD05/UART	3.3V
A33	UART5_TXD	3.3V	B33	LIO_AD06/UART	3.3V
A34	UART3_RXD	3.3V	B34	LIO_AD07/UART	3.3V
A35	UART3_TXD	3.3V	B35	LS2K_GPIO1	3.3V
A36	UART4_RXD	3.3V	B36	LS2K_GPIO2	3.3V
A37	UART4_TXD	3.3V	B37	LS2K_GPIO3	3.3V
A38	UART0_RXD	3.3V	B38	GMC1_LED2	3.3V

A39	UART0_TXD	3.3V	B39	GMC0_LED2	3.3V
A40	GMC1_LED1	3.3V	B40	GMC0_LED1	3.3V
A41	GND		B41	GND	
A42	GMC1_TRD0-	diff	B42	GMC0_TRD0-	diff
A43	GMC1_TRD0+	diff	B43	GMC0_TRD0+	diff
A44	GMC1_TRD1-	diff	B44	GMC0_TRD1-	diff
A45	GMC1_TRD1+	diff	B45	GMC0_TRD1+	diff
A46	GND		B46	GND	
A47	GMC1_TRD2-	diff	B47	GMC0_TRD2-	diff
A48	GMC1_TRD2+	diff	B48	GMC0_TRD2+	diff
A49	GMC1_TRD3-	diff	B49	GMC0_TRD3-	diff
A50	GMC1_TRD3+	diff	B50	GMC0_TRD3+	diff
A51	GND		B51	GND	
A52	LS2K_DVO1_D23	3.3V	B52	LS2K_DVO1_D16	3.3V
A53	LS2K_DVO1_D22	3.3V	B53	LS2K_DVO1_D17	3.3V
A54	LS2K_DVO1_D21	3.3V	B54	LS2K_DVO1_D18	3.3V
A55	LS2K_DVO1_D20	3.3V	B55	LS2K_DVO1_D19	3.3V
A56	LS2K_DVO1_D15	3.3V	B56	LS2K_DVO1_D06	3.3V
A57	LS2K_DVO1_D14	3.3V	B57	LS2K_DVO1_D04	3.3V
A58	LS2K_DVO1_DE	3.3V	B58	LS2K_DVO1_D07	3.3V
A59	LS2K_DVO1_CLKP	3.3V	B59	LS2K_DVO1_D05	3.3V
A60	GND		B60	GND	
A61	LS2K_DVO1_D13	3.3V	B61	LS2K_DVO1_D01	3.3V
A62	LS2K_DVO1_D12	3.3V	B62	LS2K_DVO1_D02	3.3V
A63	LS2K_DVO1_D11	3.3V	B63	LS2K_DVO1_D03	3.3V
A64	LS2K_DVO1_D10	3.3V	B64	LS2K_DVO1_D00	3.3V
A65	LS2K_DVO1_D09	3.3V	B65	LS2K_DVO1_VSYNC	3.3V
A66	LS2K_DVO1_D08	3.3V	B66	LS2K_DVO1_HSYNC	3.3V
A67	GND		B67	USB0_ID/PCIE_RSTN	3.3V
A68	PCIE1_REFCLK0_N	diff	B68	USB3_BUS_DM	3.3V
A69	PCIE1_REFCLK0_P	diff	B69	USB3_BUS_DP	3.3V
A70	GND		B70	GND	
A71	USB2_BUS_DM	diff	B71	USB_OC	3.3V
A72	USB2_BUS_DP	diff	B72	USB1_BUS_DP	diff
A73	PCIE0_PRSTN0	3.3V	B73	USB1_BUS_DM	diff
A74	GND		B74	GND	
A75	PCIE00_TX0N	diff	B75	PCIE0_REFCLK0_N	diff
A76	PCIE00_TX0P	diff	B76	PCIE0_REFCLK0_P	diff
A77	GND		B77	GND	
A78	PCIE00_TX1N	diff	B78	PCIE00_RX0P	diff
A79	PCIE00_TX1P	diff	B79	PCIE00_RX0N	diff
A80	GND		B80	GND	
A81	GND		B81	GND	

A82	PCIE00_TX2N	diff	B82	PCIE00_RX1P	diff
A83	PCIE00_TX2P	diff	B83	PCIE00_RX1N	diff
A84	GND		B84	GND	
A85	PCIE00_TX3N	diff	B85	PCIE00_RX2P	diff
A86	PCIE00_TX3P	diff	B86	PCIE00_RX2N	diff
A87	GND		B87	GND	
A88	PCIE11_TX0P	diff	B88	PCIE00_RX3P	diff
A89	PCIE11_TX0N	diff	B89	PCIE00_RX3N	diff
A90	GND		B90	GND	
A91	PCIE11_TX1P	diff	B91	PCIE11_RX0P	diff
A92	PCIE11_TX1N	diff	B92	PCIE11_RX0N	diff
A93	GND		B93	GND	
A94	PCIE1_PRSTN1	diff	B94	PCIE11_RX1P	diff
A95	PCIE1_PRSTN0	diff	B95	PCIE11_RX1N	diff
A96	USB0_PWR	5.0V	B96	GND	
A97	USB0_OC	3.3V	B97	SATA_RX_P	diff
A98	USB0_DP	diff	B98	SATA_RX_N	diff
A99	USB0_DM	diff	B99	GND	
A100	GND		B100	GND	
A101	PCIE1_REFCLK1_P	diff	B101	SATA_TX_P	diff
A102	PCIE1_REFCLK1_N	diff	B102	SATA_TX_N	diff
A103	RTC_POWER	3.3V	B103	GND	
A104	VDD_VIN	5~12V	B104	VDD_VIN	5~12V
A105	VDD_VIN	5~12V	B105	VDD_VIN	5~12V
A106	VDD_VIN	5~12V	B106	VDD_VIN	5~12V
A107	VDD_VIN	5~12V	B107	VDD_VIN	5~12V
A108	VDD_VIN	5~12V	B108	VDD_VIN	5~12V
A109	VDD_VIN	5~12V	B109	VDD_VIN	5~12V
A110	GND		B110	GND	

二，修订记录

1，第一版。D2021.06.04

修订 1：D2021.10.18

修订部分指标，更改版本号为 V120。

修订 2：D2022.04.06

更改结构尺寸示意图